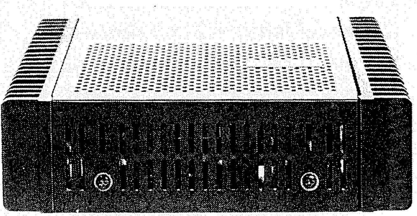
Service Manual

ORDER NO.
CRT-491-0


(Hideaway Unit Section)

COMPONENT CAR STEREO COMPACT DISC PLAYER WITH CONTROL AMPLIFIER

CDX-P1 US, ES, EW

COMPACT
disc
DIGITAL AUDIO

- For the circuit descriptions, please refer to the CDX-1 service manual (CRT-487-0).

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TEL: [03] 580-9911

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SPECIFICATIONS

General

System	Motor vehicle compact disc digital audio system
Disc	Diameter: 120mm
	Thickness: 1.2mm
	Maximum playing time: Over 60 minutes (stereo)
	Linear velocity: 1.2 ~ 1.4m/sec.
	Rotation direction: Counterclockwise
Signal format	Sampling frequency: 44.1 kHz
	Number of quantization bits: 16; linear
	Transmission bit rate: 4.3218 Mbit/sec.
	Modulation system: EFM
	Error correction system: CIRC
	Pre-emphasis: 50/15μsec.
Laser	Semiconductor laser: wavelength 780nm
Power requirements	14.4V DC (10.8 ~ 15.6V possible)
Power consumption	19W
Weight	Player section: 2.2kg (4.8 lbs.)
	Hideaway unit section: 1.7kg (3.7 lbs.)
Dimensions	Player section: 180(W) x 50(H) x 165(D)mm
	[7-1/8(W) x 2(H) x 6-1/2(D) in.]
	Hideaway unit section: 180(W) x 50(H) x 165(D)mm
	[7-1/8(W) x 2(H) x 6-1/2(D) in.]

Audio

Frequency characteristics	10 ~ 20,000Hz (±1 dB)
Signal-to-noise ratio	90 dB (1 kHz) (IHF-A network)
Dynamic range	90 dB (1 kHz)
Wow and flutter	Below measurement range
Distortion factor	0.005% (1 kHz, 0 dB)
Maximum output voltage	300mV (1 kHz, 0 dB)
Number of channels	2 (stereo)
Tone controls (bass)	±10 dB (100 Hz)
(Treble)	±10 dB (10 kHz)
Output impedance	1kΩ

These specifications were determined and are presented in accordance with specification standards established by the Ad Hoc Committee of Car Stereo Manufacturers.

Note:
Specifications and the design are subject to possible modification without notice due to improvements.

Noncontact Optical Pickup

A slight laser beam generated by the optical pickup strikes the signal surface of the disc. The reflected beam is then sent to a photodiode which reads the digital signals picked up from the disc. Since signals are read without contacting the surface of the medium, needle generated friction as in conventional phonograph systems and the accompanying hiss are eliminated. Also, since the disc itself is coated with clear plastic, the signal surface is protected from the effects of dust, finger smudges and dirt.

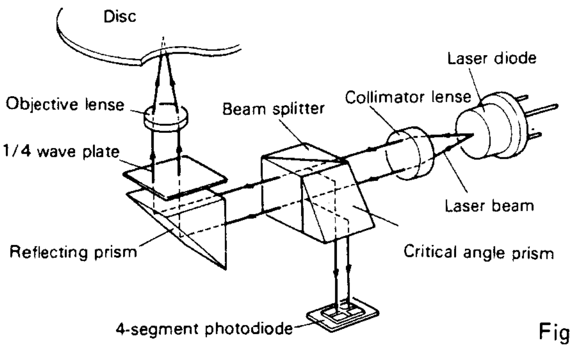


Fig. 1

Pickup Block Diagram

1. SAFETY INFORMATION (CDX-P1/US)

1. Safety Precautions for those who Service this Unit.

- Follow the adjustment steps (see pages 28 through 35) in the service manual when servicing this unit. Whe checking or adjusting the emitting power of the laser diode exercise caution in order to get safe, reliable results.

Caution:

1. During repair or tests, minimum distance of 13cm from the focus lens must be kept.
2. During repair or tests, do not view laser beam for 10 seconds or longer.

2. A "CERTIFICATION AND IDENTIFICATION" label is affixed to the bottom of the player. (Fig. 2-1, 2)

- Two screws are affixed to the bottom of the unit to secure the mechanism during transport. Be sure to remove these screws before installation of the player. (Fig. 2-1)

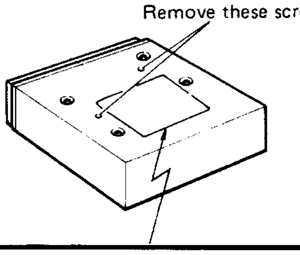
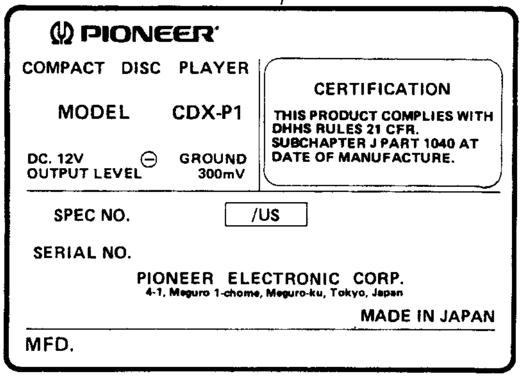


Fig. 2-1


PIONEER

COMPACT DISC PLAYER

MODEL CDX-P1

DC. 12V ⊖ GROUND
OUTPUT LEVEL 300mV

CERTIFICATION

THIS PRODUCT COMPLIES WITH DHHS RULES 21 CFR. SUBCHAPTER J PART 1040 AT DATE OF MANUFACTURE.

SPEC NO. /US

SERIAL NO.

PIONEER ELECTRONIC CORP.
4-1, Meguro 1-chome, Meguro-ku, Tokyo, Japan
MADE IN JAPAN

MFD.

Fig. 2-2

4. Specifications of Laser Diode

Specifications of laser radiation fields to which human access is possible during service.

Wavelength	=	780 nanometers
Radiant power	=	55.3 microwatts (Through a circular aperture stop having a diameter of 80 millimeters)
		0.44 microwatts (Through a circular aperture stop having a diameter of 7 millimeters)

3. The WARNING label is attached to the mechanism unit plate unit and right side of the case. (Fig. 3-1, 2)

DANGER

INVISIBLE LASER RADIATION WHEN OPEN AND INTERLOCK FAILED OR DEFEATED.
AVOID DIRECT EXPOSURE TO BEAM.

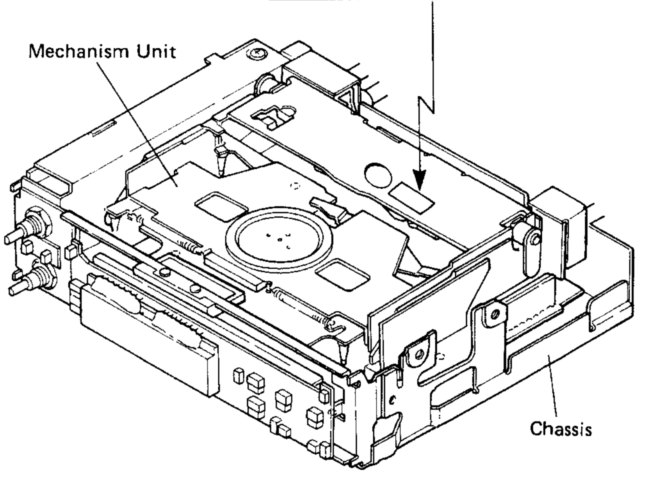


Fig. 3-1

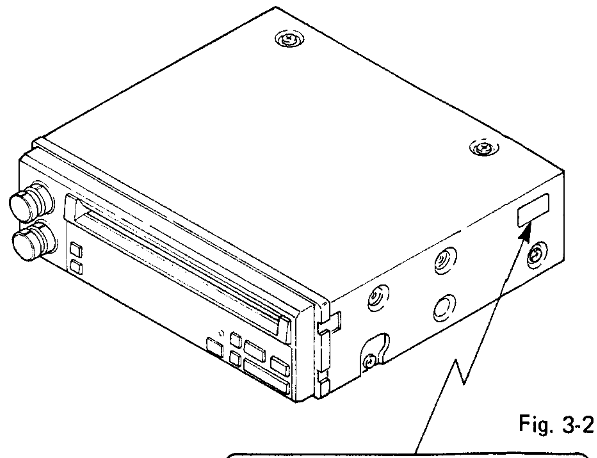


Fig. 3-2

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2. SAFETY INFORMATION (CDX-P1/EW)

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Caution:

1. During repair or tests, minimum distance of 13cm from the focus lens must be kept.
2. During repair or tests, do not view laser beam for 10 seconds or longer.

2. A "CLASS 1 LASER PRODUCT" label is affixed to the bottom of the player. (Fig. 4-1, 2)

- Two screws are affixed to the bottom of the unit to secure the mechanism during transport. Be sure to remove these screws before installation of the player. (Fig. 4-2)

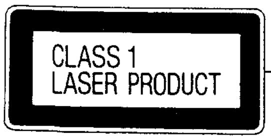

Fig. 4-1

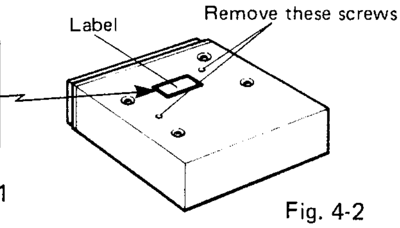

Fig. 4-2

3. The triangular label is attached to the mechanism unit plate unit (Fig. 5)

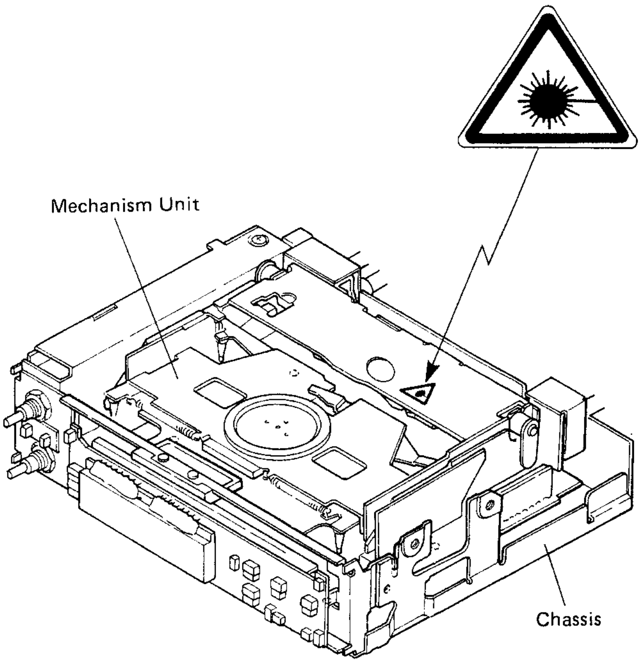

Fig. 5

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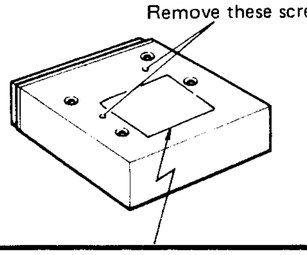
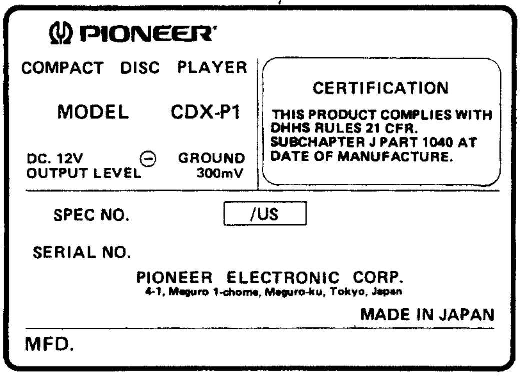


Fig. 2-1



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COMPACT DISC PLAYER

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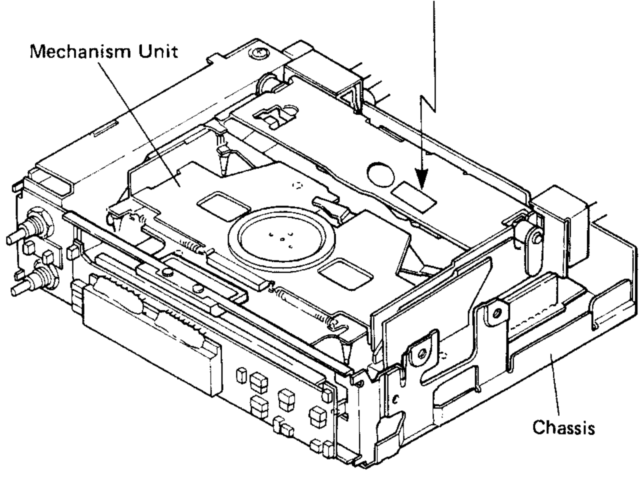

Fig. 3-1

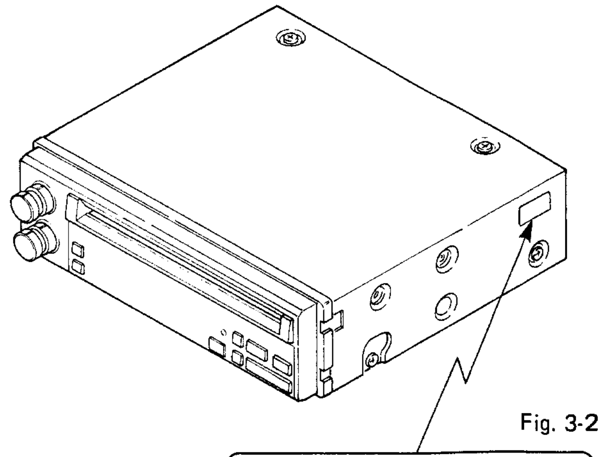

Fig. 3-2

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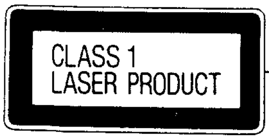
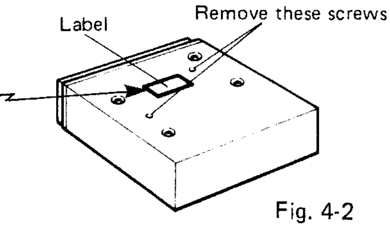


Fig. 4-1



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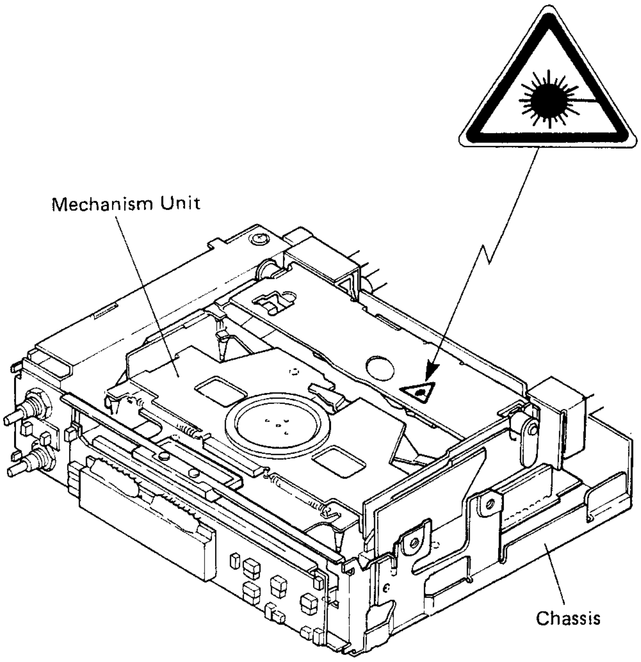

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0.44 microwatts
(Through a circular aperture stop having a diameter of 7 millimeters)

3. NAME OF PARTS AND THEIR FUNCTIONS

3.1 PLAYER SECTION

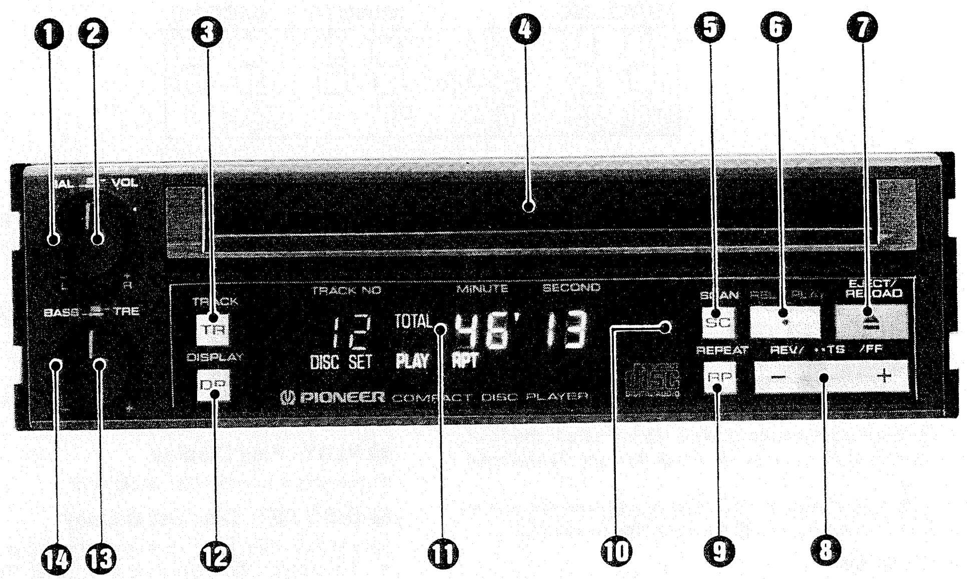


Fig. 6

❶ Balance Control

❷ Volume Control

❸ Track Number Search Button

Used to find the start point of a selection. Pressing this button once will increase the track number shown on the display by one, while holding it down will cause the track number to be continuously incremented at high speed.

❹ Disc Insert Slot

With the side of the disc containing the label (with the names of the selections) facing up, start the disc into the insert slot. The auto loading mechanism will then take over to set the disc and begin play.

❺ Music Scan Button

Press to sequentially search for the beginning of each selection and play the first ten seconds. When the selection being searched for is found, pressing the release button returns to normal play. Even if the unit is left in the scan function, normal play will be resumed when the beginning of the selection from which music scan was initiated is reached.

❻ Release/Play Button

Press to cancel music scan, music repeat or either of the high speed functions during their respective operation. This button is also pressed to temporarily suspend disc play in standby mode, and pressing again will resume disc play.

❼ Eject/Reload Button

Press to eject the disc during play, and press once again to reset.

❽ High Speed Forward (+)/High Speed Reverse (−) Buttons

Pressing the (+) button will advance the disc at high speed, while pressing the (−) button will enable high speed reverse. To perform track search, press either one of these buttons twice.

❾ Music Repeat Button

Press to continually repeat the selection being played. This function is cancelled either by pressing again or by pressing the release button. When this function is not being used, the disc will continually play from beginning to end.

❿ Clear Button

Should abnormalities occur during disc play (such as improper display), press this button with a thin pointed object. The unit will return to normal operations after a few seconds.

⓫ Display

⓬ Display Select Button

Switches the contents of the display from A to B to C with each respective press.

A: TOTAL and REMAIN disappear from the display and the track number being played together with the elapsed time of that selection will be shown.

B: TOTAL illuminates on the display and the total number of selections included on the disc together with the total play time of the disc will be shown.

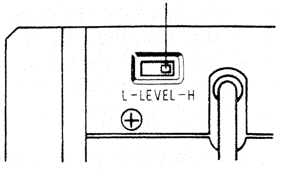
C: REMAIN illuminates on the display and the number of selections remaining together with play time remaining will be shown.

⓭ Treble Control

⓮ Bass Control

- Each push button features both an electronic beep signal and illuminated display to allow dual confirmation of proper operation.
- A level switch is located on the back of the hideaway unit. Usually this switch is kept in the H (high) position. Setting the switch to the L (low) position will decrease the power level by 6 dB.

Level switch usually left in the H (high) position.



Hideaway unit section

Fig. 7

3.2 READING THE DISPLAYS

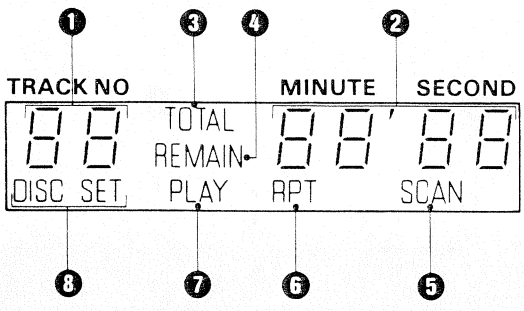


Fig. 8

❶❷ 8888'88 : Track, Time Display

Each time the display select button is pressed the contents of the display are switched from A to B to C respectively.

A: When TOTAL ❸ and REMAIN ❹ disappear from the display, ❶ will show the track number being played and ❷ the elapsed time of that track.
B: When TOTAL ❸ illuminates on the display, ❶ will show the total number of selections included on the disc together and ❷ the total play time of the disc.
C: When REMAIN ❹ illuminates on the display, ❶ will show the number of selections remaining and ❷ the play time remaining.

❸ TOTAL : Total Display

The display select button is pressed until this indicator illuminates on the display. The total number of selections included on the disc is indicated by ❶ and the total play time of the disc is indicated by ❷.

❹ REMAIN : Remain Display

The display select button is pressed until this indicator illuminates on the display. The number of selections remaining is indicated by ❶ and the play time remaining is indicated by ❷.

❺ SCAN : Music Scan Display

Illuminates when the scan button is pressed to indicate that the scan function is operational.

❻ RPT : Music Repeat Display

Illuminates when the music repeat button is pressed to indicate that the repeat function is operational.

❼ PLAY : Play Display

Illuminates while the disc is playing.

❽ DISC SET : Disc Set Display

Illuminates when the disc is set in the player.

- To protect the semiconductor laser from damage, this unit contains a feature which automatically stops disc play when the ambient temperature rises past a certain level. When this occurs, ❶ and ❷ will show HHHHHH . Eject the disc from the unit using the eject button and wait until the temperature returns to normal.
- When a space of a few seconds exists between the selections of the disc being used, ❷ will show -'02, -'01 when the spaces are passed.

3.3 OPERATION

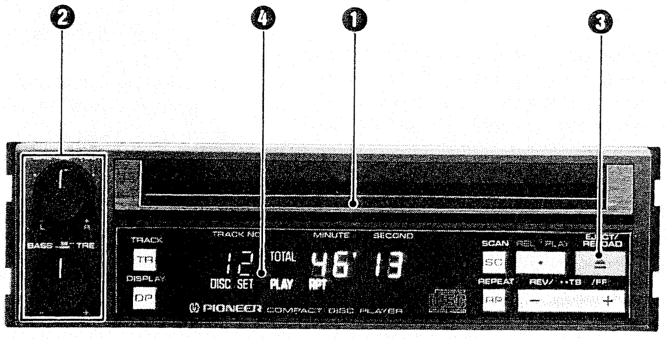


Fig. 9

1. With the side of the disc with the label (with the names of the selections) facing up, start the disc into the insert slot ❶. The auto loading mechanism will then take over to set the disc and begin play.
2. Adjust the volume, balance, bass and treble ❷ to the desired settings.
3. To stop disc play or to change discs, press the eject/reload button ❸. Pressing again will start play from the first selection of the disc in the unit.

- Illumination of DISC SET on the display ❹ indicates that a disc is set in the unit. Note that attempting to insert another disc in this condition can cause damage to the discs and/or mechanical failure.
- Never attempt to stack two discs together and insert them into the unit at the same time. This can cause mechanical failure of the unit.

• Track Number Search

This operation is convenient for skipping past a number of tracks to a specific selection.

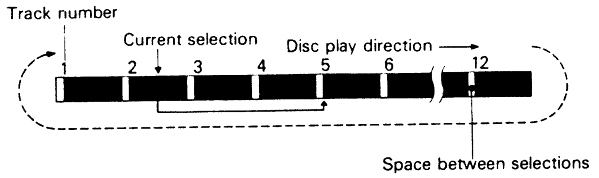

Track number
Current selection
Disc play direction →
1
2
3
4
5
6
12
Space between selections

Fig. 10

Moving from Play in Selection 2 to Selection 5

Press the track number search button until the display shows track number 5.

• Music Scan

This operation allows a quick review of the selections on the disc. The beginning of each selection is sequentially located and played for 10 seconds before moving to the next selection.
Once the beginning of all the selections on the disc have been played and the selection from which this operation was initiated is returned to, music scan is released and normal disc play resumes.

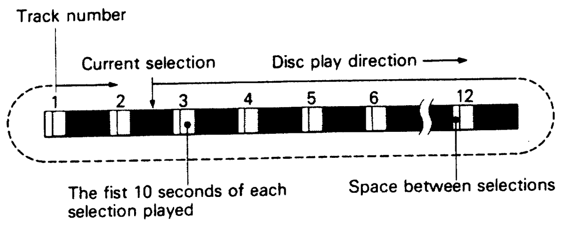

Track number
Current selection
Disc play direction →
1
2
3
4
5
6
12
The fist 10 seconds of each selection played
Space between selections

Fig. 11

Moving from Play in Selection 2 to Search for Another Selection

1. Press the music scan button (SCAN illuminates on the display).
2. When the beginning of the desired selection is playing, press the release button to cancel music scan and resume normal disc play.

- Music scan can be cancelled at any time during its operation by pressing the release button.

• Music Repeat

This operation can be used to replay a certain selection as many times as desired.

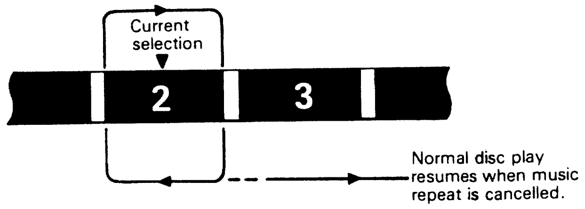

Current selection
2
3
Normal disc play resumes when music repeat is cancelled.

Fig. 12

Listening to Selection 2 Repeatedly

Press the music repeat button during play of selection 2 (RPT illuminates on the display). Selection 2 will then be repeated until music repeat is cancelled.

- Music repeat can be canceled at any time during its operation by pressing the release button or the music repeat button.
- When this function is not being used, the disc will continually play from beginning to end.

• Track Search

This operation is useful for returning to the beginning of the current selection or jumping to the beginning of the next selection.

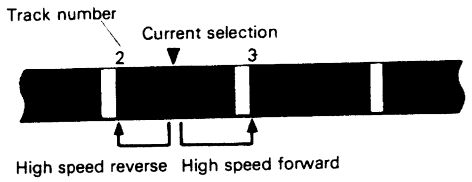

Track number
Current selection
2
3
High speed reverse
High speed forward

Fig. 13

Listening to Selection 2 One More Time

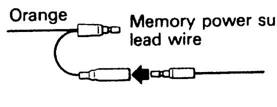
Press the high speed reverse button (−) twice. Play will automatically resume from the beginning of selection 2.

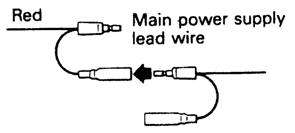
Skipping Over Selection 2 to Listen to Selection 3

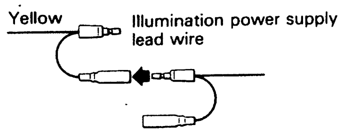
Press the high speed forward button (+) twice. Play will automatically start from the beginning of selection 3.

4. CONNECTION

- Before making final connections, make temporary connections then operate the unit to check for any connecting cord problems.
- Connect the red and black connectors of the player to the respective red and black connectors of the hideaway unit, and securely tighten the retaining rings.
- Refer to the owner's manual for details on connecting the various cords of the main amp and other units then make connections correctly.
- Be sure to correctly connect the memory power supply lead (orange) and main power supply lead (red) as specified. If the connections are made incorrectly or forgotten, this unit will not work at all.
- Don't pass the memory power supply lead through a hole into the engine compartment to connect to the battery. This will damage the lead insulation and cause a very dangerous short.
- If you should encounter more than two lead wires of the same color, when wiring connections, it will be convenient to wire them together, as shown in the following diagram.


Orange
Memory power supply lead wire


Red
Main power supply lead wire


Yellow
Illumination power supply lead wire

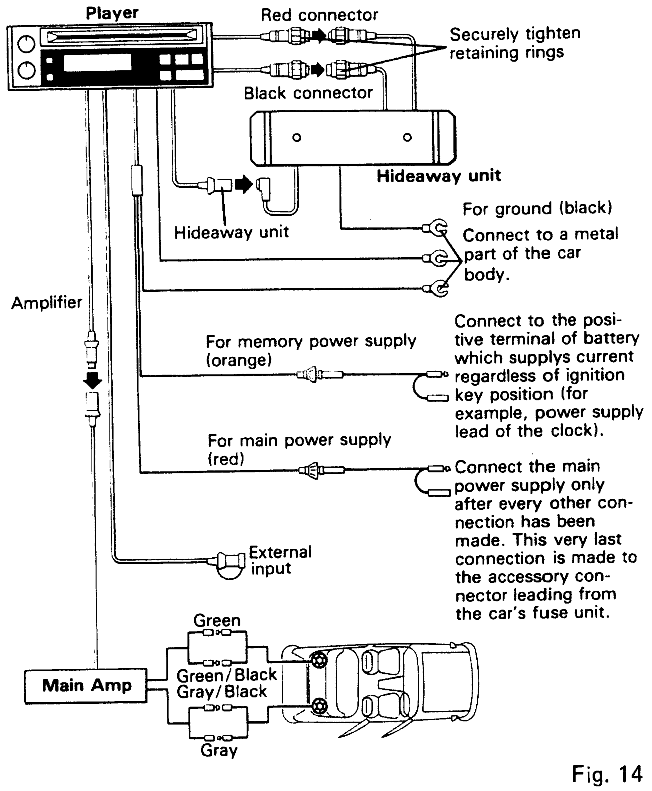

Player
Red connector
Securely tighten retaining rings
Black connector
Hideaway unit
Hideaway unit
For ground (black)
Connect to a metal part of the car body.
Amplifier
For memory power supply (orange)
Connect to the positive terminal of battery which supplys current regardless of ignition key position (for example, power supply lead of the clock).
For main power supply (red)
Connect the main power supply only after every other connection has been made. This very last connection is made to the accessory connector leading from the car's fuse unit.
External input
Green
Green/Black
Gray/Black
Gray
Main Amp

Fig. 14

5. LEVEL DIAGRAM

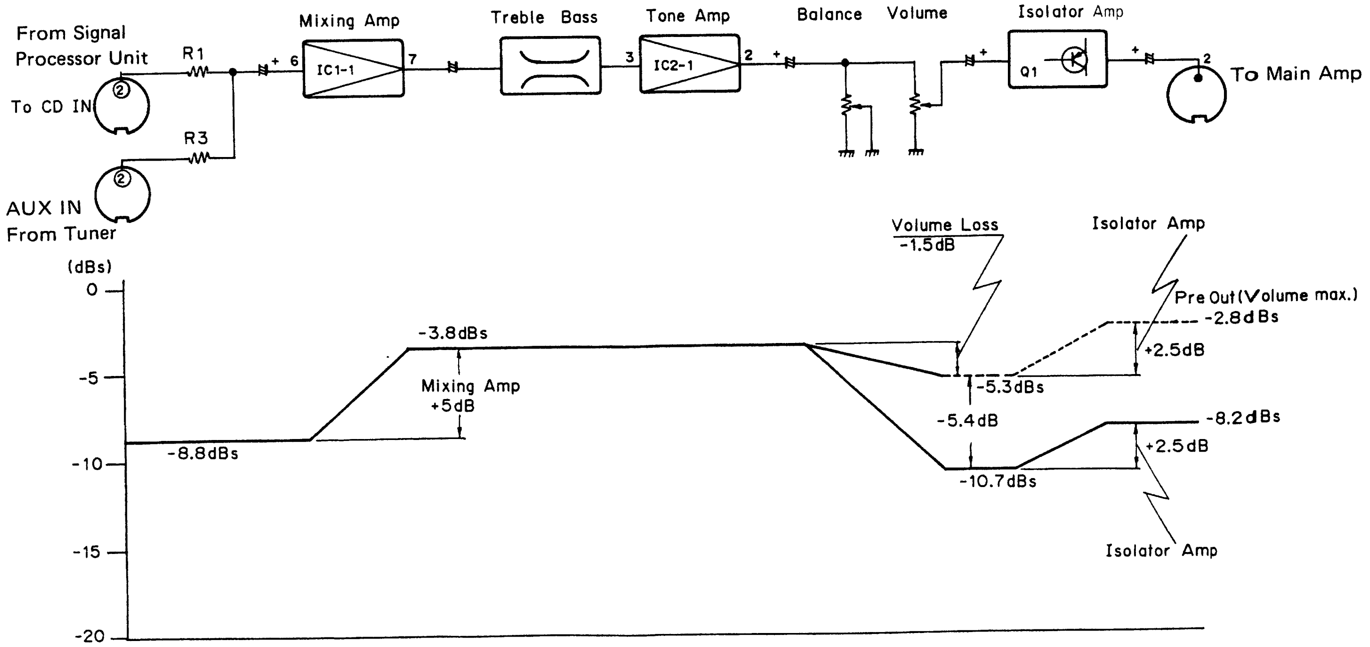

From Signal Processor Unit
R1
To CD IN
②
R3
AUX IN From Tuner
②
Mixing Amp
IC1-1
6
7
Treble Bass
Tone Amp
IC2-1
3
2
Balance
Volume
Isolator Amp
Q1
2
To Main Amp
(dBs)
0
-5
-10
-15
-20
-8.8dBs
-3.8dBs
Mixing Amp +5dB
Volume Loss -1.5dB
-5.3dBs
-5.4dB
-10.7dBs
Isolator Amp
Pre Out (Volume max.)
-2.8dBs
+2.5dB
-8.2dBs
+2.5dB
Isolator Amp

Fig. 15

6. BLOCK DIAGRAM

- **Player Section**

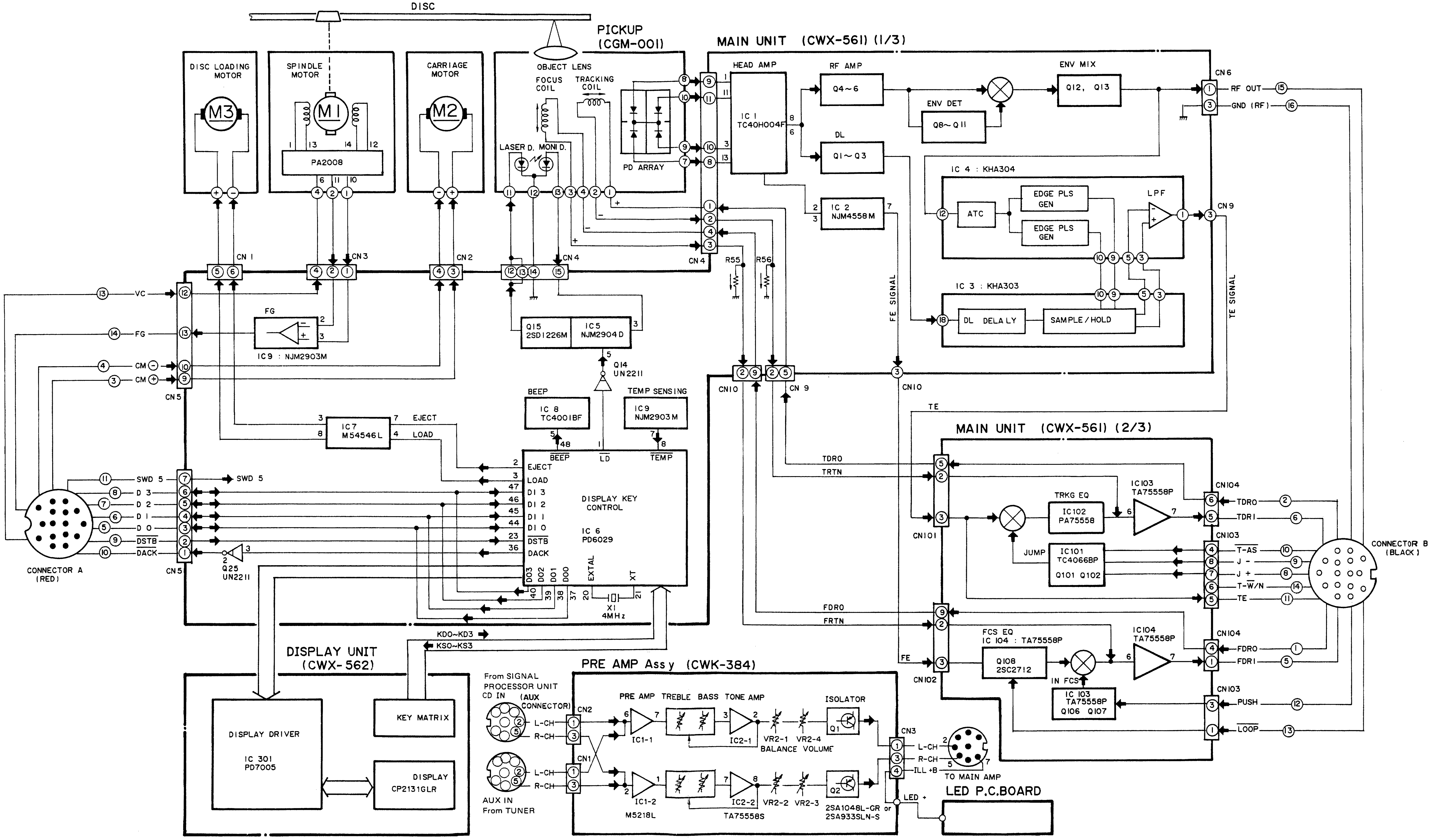

DISC
PICKUP (CGM-001)
MAIN UNIT (CWX-561) (1/3)
DISC LOADING MOTOR
M3
SPINDLE MOTOR
M1
PA2008
CARRIAGE MOTOR
M2
OBJECT LENS
FOCUS COIL
TRACKING COIL
LASER D.
MONI D.
PD ARRAY
HEAD AMP
IC 1 TC40H004F
RF AMP
Q4~6
DL
Q1~Q3
ENV MIX
Q12, Q13
ENV DET
Q8~Q11
IC 2 NJM4558M
IC 4 : KHA304
ATC
EDGE PLS GEN
EDGE PLS GEN
LPF
IC 3 : KHA303
DL DELALY
SAMPLE/HOLD
CN6
RF OUT
GND (RF)
CN9
TE SIGNAL
FE SIGNAL
R55
R56
CN1
CN2
CN3
CN4
CN5
CN10
CN 9
VC
FG
CM⊖
CM⊕
IC9 : NJM2903M
Q15 2SD1226M
IC5 NJM2904D
Q14 UN2211
BEEP
IC 8 TC4001BF
TEMP SENSING
IC9 NJM2903M
IC7 M54546L
EJECT
LOAD
SWD 5
D 3
D 2
D 1
D 0
DSTB
DACK
Q25 UN2211
CONNECTOR A (RED)
DISPLAY KEY CONTROL
IC 6 PD6029
EJECT
LOAD
DI 3
DI 2
DI 1
DI 0
DSTB
DACK
DO3 DO2 DO1 DO0
EXTAL
XT
X1 4MHz
LD
TEMP
KD0~KD3
KS0~KS3
DISPLAY UNIT (CWX-562)
DISPLAY DRIVER
IC 301 PD7005
KEY MATRIX
DISPLAY CP2131GLR
MAIN UNIT (CWX-561) (2/3)
TE
TDRO
TRTN
CN101
TRKG EQ
IC102 PA75558
IC103 TA75558P
JUMP
IC101 TC4066BP
Q101 Q102
CN104
CN103
TDRO
TDRI
T-AS
J -
J +
T-W/N
TE
CONNECTOR B (BLACK)
FDRO
FRTN
FE
CN102
FCS EQ
IC 104 : TA75558P
Q108 2SC2712
IN FCS
IC 103 TA75558P
Q106 Q107
IC104 TA75558P
FDRO
FDRI
PUSH
LOOP
PRE AMP Assy (CWK-384)
From SIGNAL PROCESSOR UNIT
CD IN (AUX CONNECTOR)
L-CH
R-CH
AUX IN
From TUNER
PRE AMP
TREBLE
BASS
TONE AMP
ISOLATOR
IC1-1
IC1-2
M5218L
IC2-1
IC2-2
TA75558S
VR2-1
VR2-4
VR2-2
VR2-3
BALANCE
VOLUME
Q1
Q2
2SA1048L-GR or 2SA933SLN-S
CN3
L-CH
R-CH
ILL +B
LED +
TO MAIN AMP
LED P.C.BOARD

Fig. 16

- **Hideaway Unit Section**

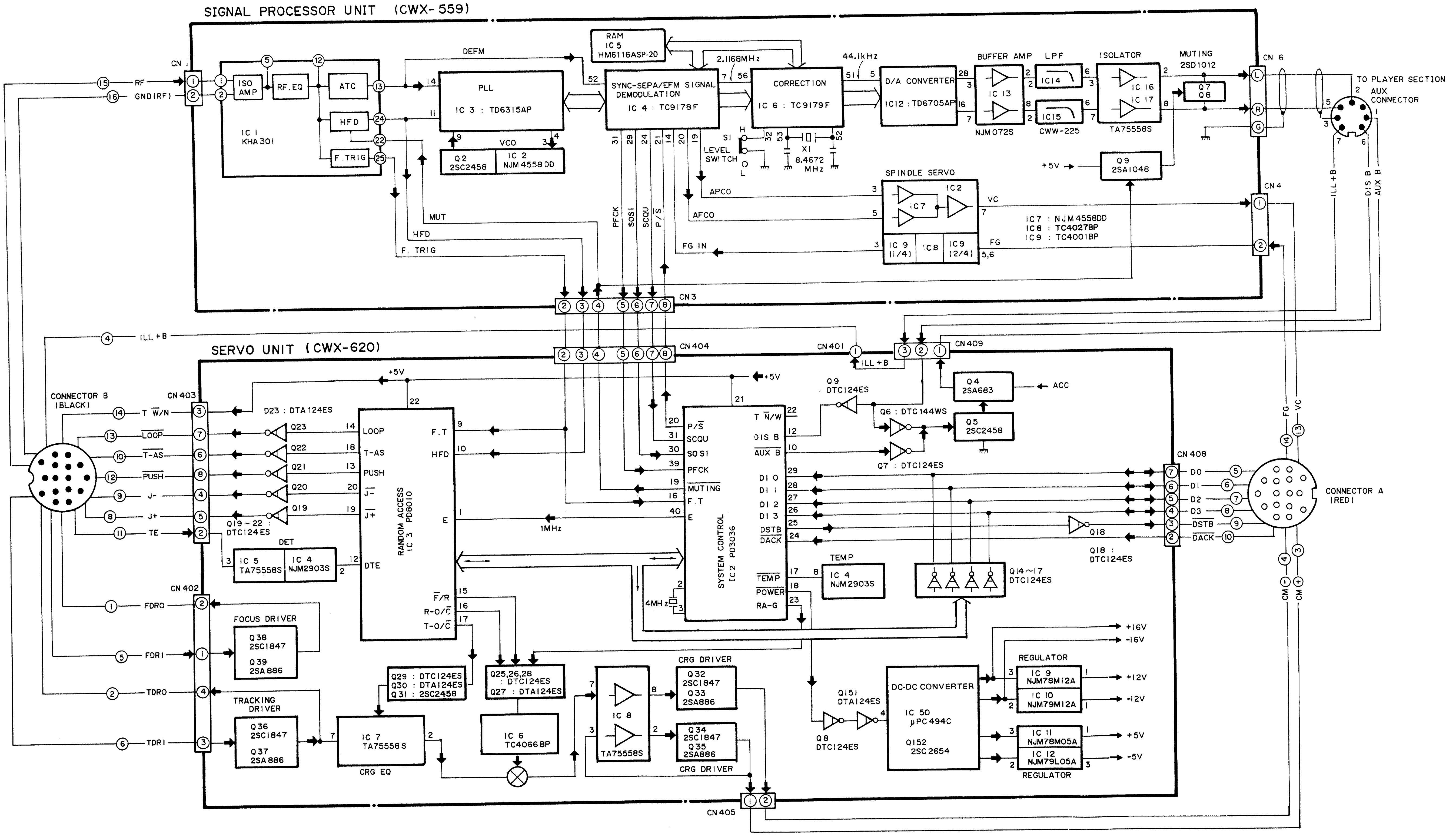

SIGNAL PROCESSOR UNIT (CWX-559)
CN 1
RF
GND(RF)
ISO AMP
RF.EQ
ATC
HFD
F.TRIG
IC 1 KHA301
DEFM
PLL
IC 3 : TD6315AP
VCO
Q2 2SC2458
IC 2 NJM4558DD
RAM IC 5 HM6116ASP-20
2.1168MHz
SYNC-SEPA/EFM SIGNAL DEMODULATION
IC 4 : TC9178F
CORRECTION
IC 6 : TC9179F
44.1kHz
D/A CONVERTER
IC12 : TD6705AP
BUFFER AMP
IC 13
NJM072S
LPF
IC14
IC15
CWW-225
ISOLATOR
IC 16
IC 17
TA75558S
MUTING
2SD1012
Q7
Q8
Q9
2SA1048
+5V
CN 6
TO PLAYER SECTION
AUX CONNECTOR
LEVEL SWITCH
X1 8.4672 MHz
SPINDLE SERVO
APCO
AFCO
FG IN
IC2
IC7
IC 9 (1/4)
IC8
IC9 (2/4)
VC
FG
IC7 : NJM4558DD
IC8 : TC4027BP
IC9 : TC4001BP
CN 4
ILL+B
DIS B
AUX B
MUT
HFD
F. TRIG
PFCK
SOSI
SCQU
P/S
CN3
CN 404
CN 401
CN 409
ILL+B
SERVO UNIT (CWX-620)
CONNECTOR B (BLACK)
CN 403
T W/N
LOOP
T-AS
PUSH
J-
J+
TE
D23 : DTA124ES
Q23
Q22
Q21
Q20
Q19
Q19 ~ 22 : DTC124ES
DET
IC 5 TA75558S
IC 4 NJM2903S
DTE
RANDOM ACCESS IC 3 PD8010
F.T
HFD
E
F/R
R-O/C
T-O/C
1MHz
+5V
SYSTEM CONTROL IC 2 PD3036
P/S
SCQU
SOSI
PFCK
MUTING
F.T
E
T N/W
DIS B
AUX B
DI 0
DI 1
DI 2
DI 3
DSTB
DACK
TEMP
POWER
RA-G
4MHz
TEMP
IC 4 NJM2903S
Q14~17 DTC124ES
Q9 DTC124ES
Q6 : DTC144WS
Q7 : DTC124ES
Q4 2SA683
ACC
Q5 2SC2458
CN 408
Q18
Q18 : DTC124ES
D0
D1
D2
D3
DSTB
DACK
CONNECTOR A (RED)
FG
VC
CM-
CM+
CN 402
FDRO
FDRI
TDRO
TDRI
FOCUS DRIVER
Q38 2SC1847
Q39 2SA886
TRACKING DRIVER
Q36 2SC1847
Q37 2SA886
Q29 : DTC124ES
Q30 : DTA124ES
Q31 : 2SC2458
IC 7 TA75558S
CRG EQ
Q25,26,28 : DTC124ES
Q27 : DTA124ES
IC 6 TC4066BP
IC 8
TA75558S
CRG DRIVER
Q32 2SC1847
Q33 2SA886
Q34 2SC1847
Q35 2SA886
CRG DRIVER
CN 405
Q151 DTA124ES
Q8 DTC124ES
DC-DC CONVERTER
IC 50 μPC494C
Q152 2SC2654
REGULATOR
IC 9 NJM78M12A
IC 10 NJM79M12A
IC 11 NJM78M05A
IC 12 NJM79L05A
REGULATOR
+16V
-16V
+12V
-12V
+5V
-5V

Fig. 17

6.1 POWER SUPPLY LINE

- **Player Section**

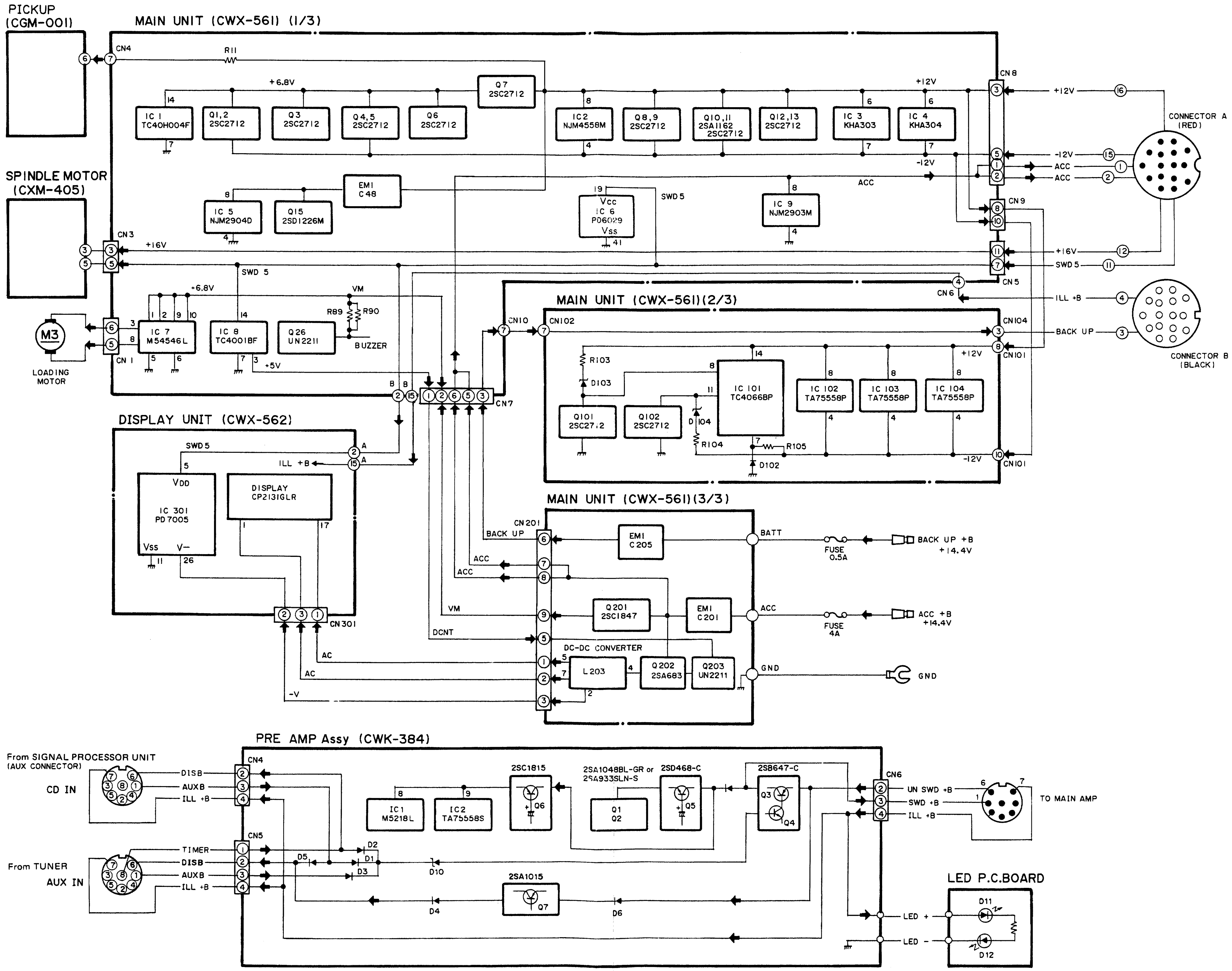

PICKUP (CGM-001)
MAIN UNIT (CWX-561) (1/3)
CN4
R11
+6.8V
Q7 2SC2712
+12V
IC 1 TC40H004F
Q1,2 2SC2712
Q3 2SC2712
Q4,5 2SC2712
Q6 2SC2712
IC2 NJM4558M
Q8,9 2SC2712
Q10,11 2SA1162 2SC2712
Q12,13 2SC2712
IC 3 KHA303
IC 4 KHA304
CN8
-12V
ACC
SPINDLE MOTOR (CXM-405)
EMI C48
IC 5 NJM2904D
Q15 2SD1226M
Vcc IC 6 PD6029 Vss
SWD 5
IC 9 NJM2903M
CN9
CN3
+16V
SWD 5
CN5
CN6
IC 7 M54546L
IC 8 TC4001BF
Q26 UN2211
R89
R90
VM
BUZZER
+5V
CN 1
M3
LOADING MOTOR
CN7
CN10
MAIN UNIT (CWX-561)(2/3)
CN102
CN104
CN101
R103
D103
Q101 2SC2712
Q102 2SC2712
D104
R104
IC 101 TC4066BP
R105
D102
IC 102 TA75558P
IC 103 TA75558P
IC 104 TA75558P
+12V
-12V
+12V
-12V
ACC
ACC
+16V
SWD 5
ILL +B
BACK UP
CONNECTOR A (RED)
CONNECTOR B (BLACK)
DISPLAY UNIT (CWX-562)
SWD 5
ILL +B
VDD
IC 301 PD7005
Vss V−
DISPLAY CP2131GLR
CN301
MAIN UNIT (CWX-561)(3/3)
CN201
BACK UP
ACC
ACC
VM
DCNT
AC
AC
−V
EMI C205
Q201 2SC1847
EMI C201
DC-DC CONVERTER
L203
Q202 2SA683
Q203 UN2211
BATT
FUSE 0.5A
BACK UP +B +14.4V
ACC
FUSE 4A
ACC +B +14.4V
GND
GND
PRE AMP Assy (CWK-384)
From SIGNAL PROCESSOR UNIT (AUX CONNECTOR)
CD IN
DISB
AUXB
ILL +B
CN4
From TUNER AUX IN
TIMER
DISB
AUXB
ILL +B
CN5
D2
D1
D3
D5
D10
IC1 M5218L
IC2 TA75558S
2SC1815
Q6
2SA1048BL-GR or 2SA933SLN-S
Q1 Q2
2SD468-C
Q5
2SB647-C
Q3
Q4
2SA1015
Q7
D4
D6
CN6
UN SWD +B
SWD +B
ILL +B
TO MAIN AMP
LED P.C.BOARD
LED +
LED −
D11
D12

Fig. 18

- **Hideaway Unit Section**

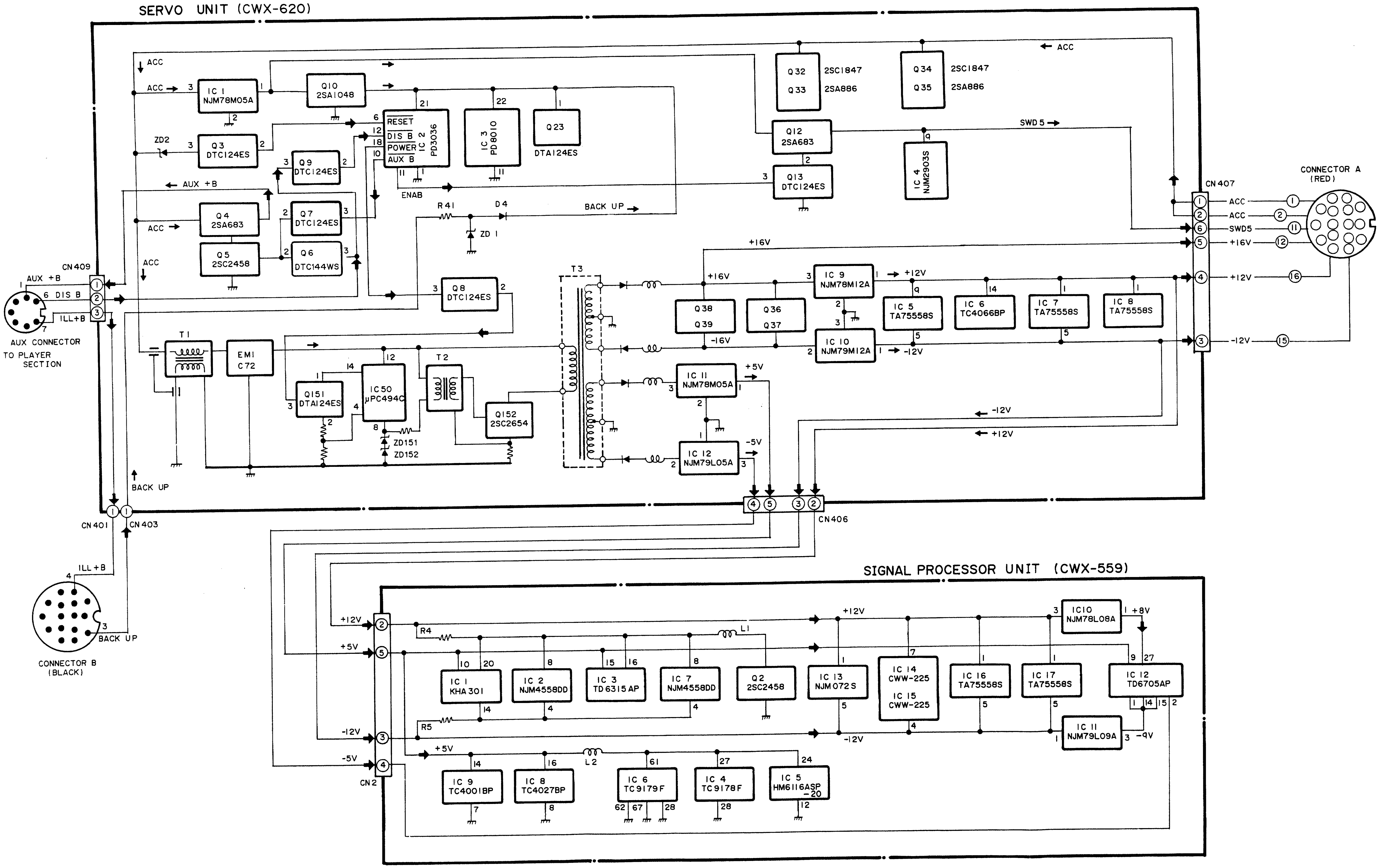

SERVO UNIT (CWX-620)
ACC
IC 1 NJM78M05A
Q10 2SA1048
IC 2 PD3036
RESET
DIS B
POWER
AUX B
ENAB
IC 3 PD8010
Q23 DTA124ES
Q3 DTC124ES
Q9 DTC124ES
ZD2
AUX +B
Q4 2SA683
Q7 DTC124ES
Q5 2SC2458
Q6 DTC144WS
R41
D4
ZD 1
BACK UP
Q8 DTC124ES
Q32 2SC1847
Q33 2SA886
Q34 2SC1847
Q35 2SA886
Q12 2SA683
Q13 DTC124ES
IC 4 NJM2903S
SWD 5
CN 407
CONNECTOR A (RED)
ACC
ACC
SWD5
+16V
+12V
-12V
CN409
AUX +B
DIS B
ILL+B
AUX CONNECTOR TO PLAYER SECTION
T1
EMI C72
T2
IC50 μPC494C
Q151 DTA124ES
Q152 2SC2654
ZD151
ZD152
T3
+16V
Q38
Q39
Q36
Q37
-16V
IC 9 NJM78M12A
IC 10 NJM79M12A
IC 5 TA75558S
IC 6 TC4066BP
IC 7 TA75558S
IC 8 TA75558S
IC 11 NJM78M05A
IC 12 NJM79L05A
+5V
-5V
-12V
+12V
CN406
CN 401
CN 403
ILL+B
BACK UP
CONNECTOR B (BLACK)
SIGNAL PROCESSOR UNIT (CWX-559)
CN2
R4
R5
L1
L2
IC 1 KHA 301
IC 2 NJM4558DD
IC 3 TD6315AP
IC 7 NJM4558DD
Q2 2SC2458
IC 13 NJM072S
IC 14 CWW-225
IC 15 CWW-225
IC 16 TA75558S
IC 17 TA75558S
IC10 NJM78L08A
+8V
IC 12 TD6705AP
IC 11 NJM79L09A
-9V
IC 9 TC4001BP
IC 8 TC4027BP
IC 6 TC9179F
IC 4 TC9178F
IC 5 HM6116ASP-20

Fig. 19

7. PARTS LOCATION

NOTE

- *For your Parts Stock Control, the fast moving items are indicated with the marks ★★ and ★.*

  ★★: GENERALLY MOVES FASTER THAN ★.

  This classification shall be adjusted by each distributor because it depends on model number, temperature, humidity, etc.

- Player Section

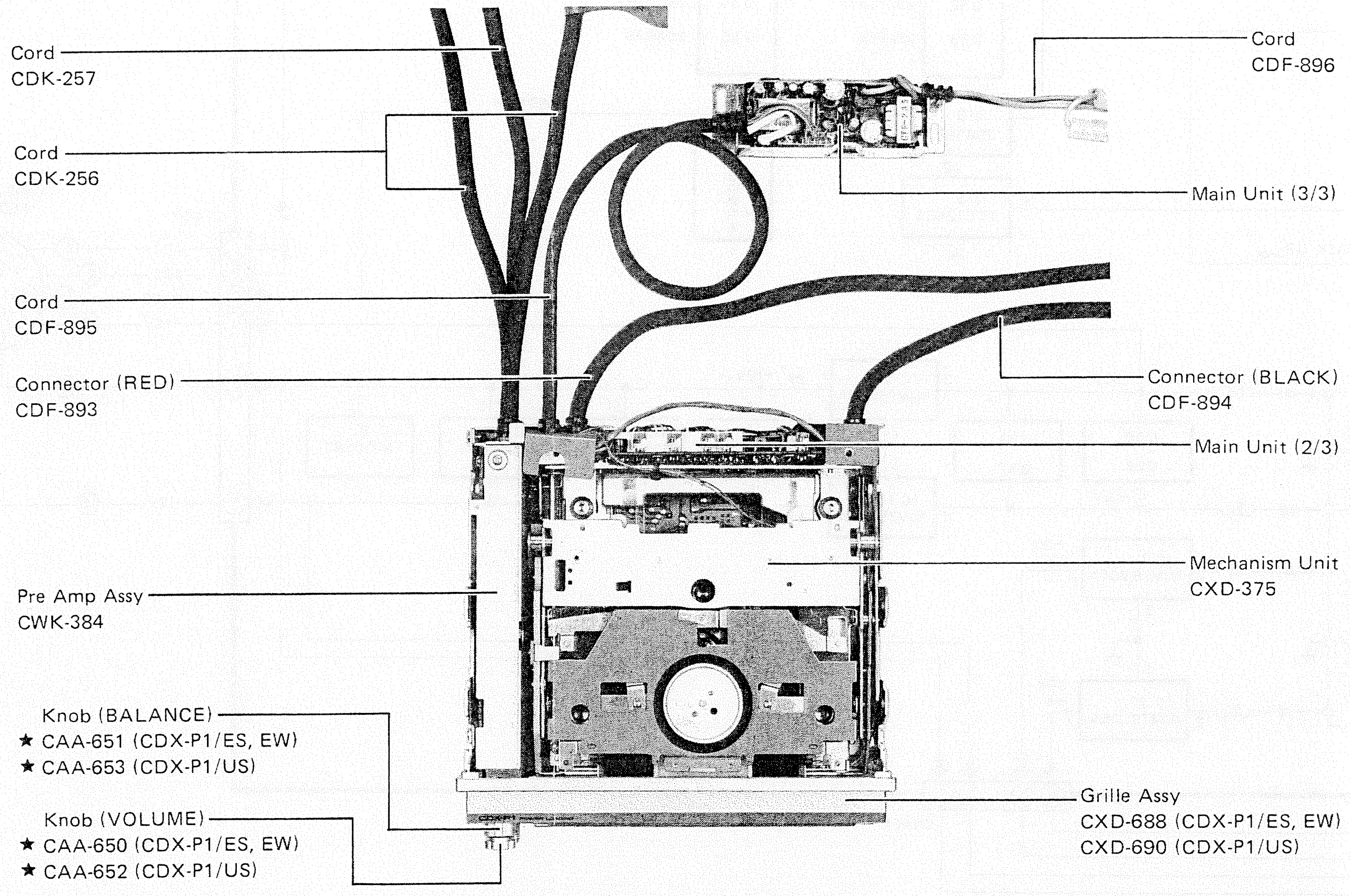

Cord
CDK-257
Cord
CDK-256
Cord
CDF-895
Connector (RED)
CDF-893
Pre Amp Assy
CWK-384
Knob (BALANCE)
★ CAA-651 (CDX-P1/ES, EW)
★ CAA-653 (CDX-P1/US)
Knob (VOLUME)
★ CAA-650 (CDX-P1/ES, EW)
★ CAA-652 (CDX-P1/US)
Cord
CDF-896
Main Unit (3/3)
Connector (BLACK)
CDF-894
Main Unit (2/3)
Mechanism Unit
CXD-375
Grille Assy
CXD-688 (CDX-P1/ES, EW)
CXD-690 (CDX-P1/US)

Fig. 20

- Hideaway Unit Section

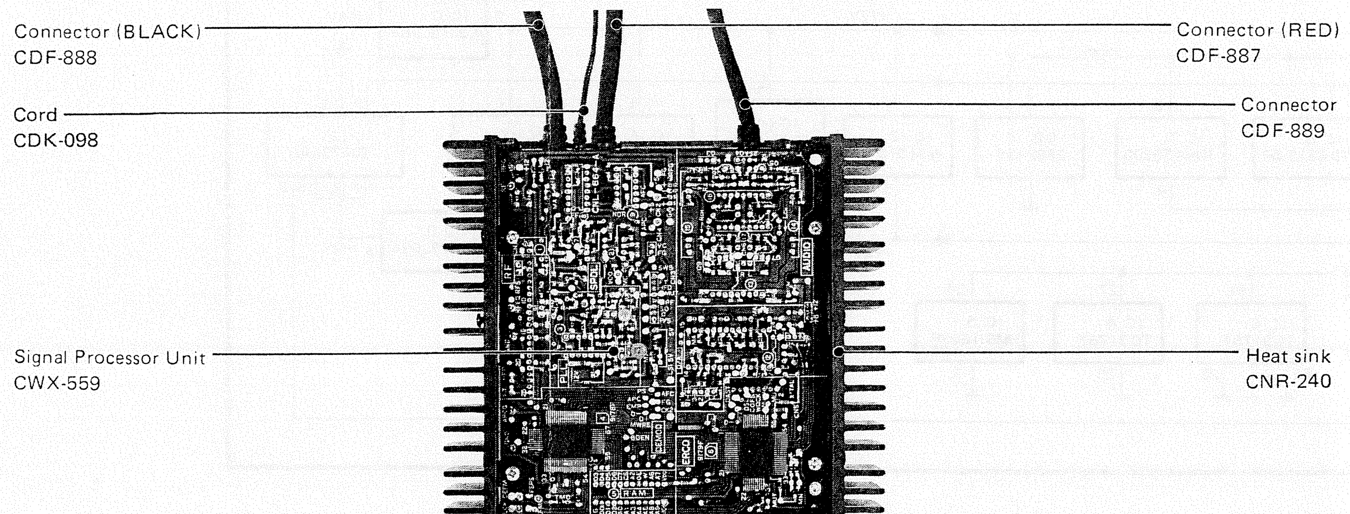

Connector (BLACK)
CDF-888
Cord
CDK-098
Signal Processor Unit
CWX-559
Connector (RED)
CDF-887
Connector
CDF-889
Heat sink
CNR-240

Fig. 21

8. DISASSEMBLY

8.1 HIDEAWAY UNIT SECTION

- **Removing the Case**

1. Remove the four screws (M3 x 8) labeled "A" which hold the case in place.

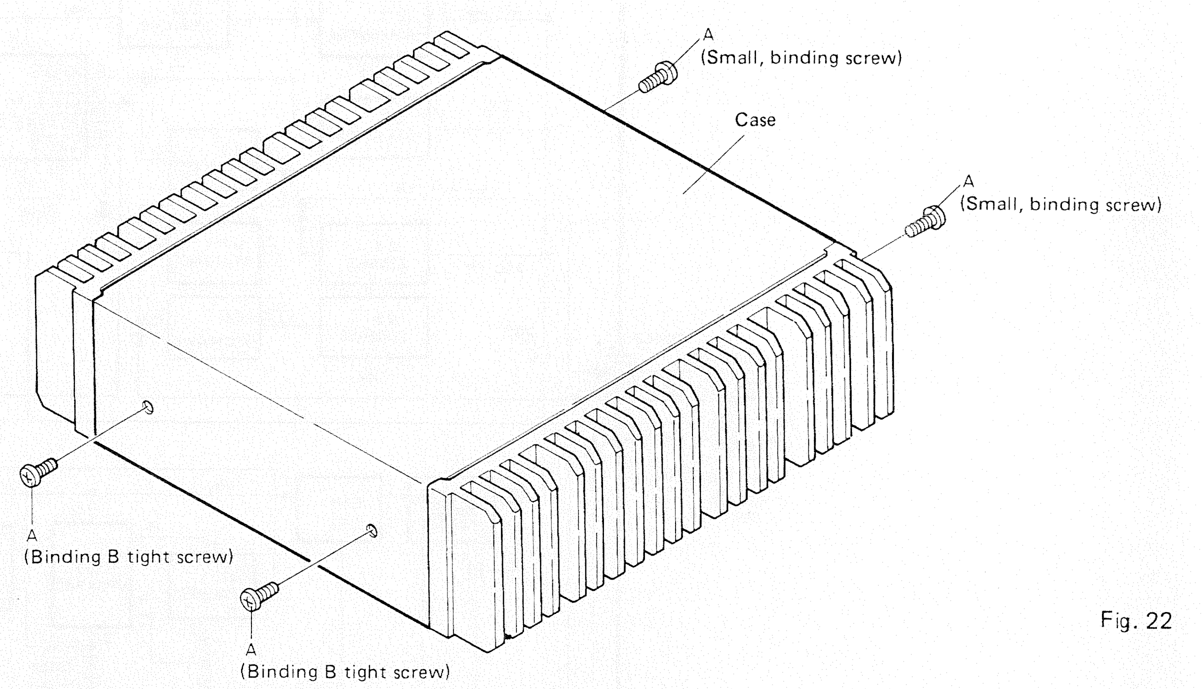

A
(Small, binding screw)
Case
A
(Small, binding screw)
A
(Binding B tight screw)
A
(Binding B tight screw)

Fig. 22

- **Removing the Chassis**

1. Remove the two screws (M3 x 8) labeled "B."

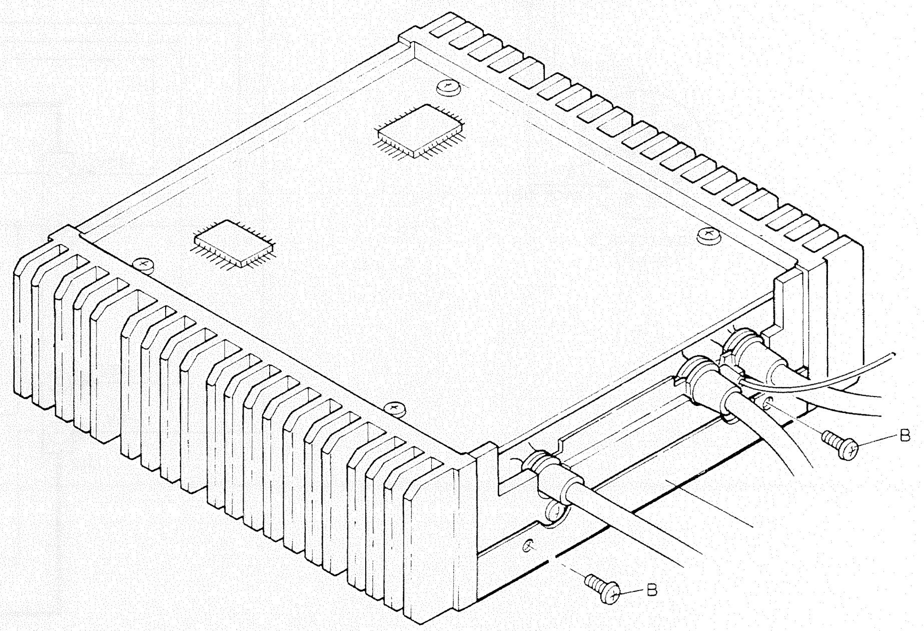


Fig. 23

Removing the Signal Processor Unit

1. Remove the four screws (M3 x 6) labeled "C."
2. Remove the connectors (8P, 3P, 2P x 2, and 6P).

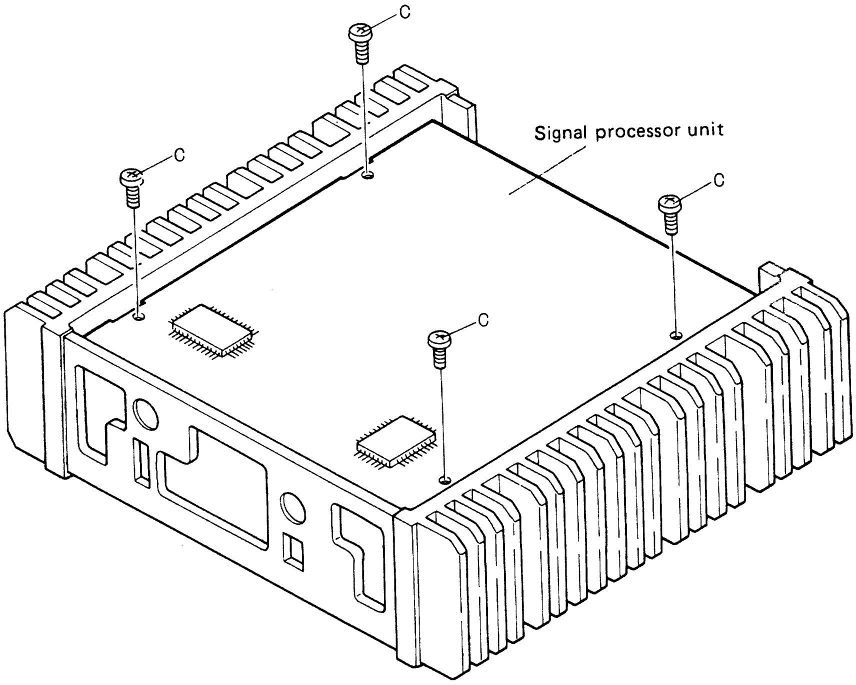

C
C
C
C
Signal processor unit

Fig. 24

Removing the Servo Unit

1. Remove the ten screws labeled "D" (M3 x 10), "E" (M3 x 8), and "F" (M3 x 6).
2. The unit will lift out in the direction indicated by the arrow.

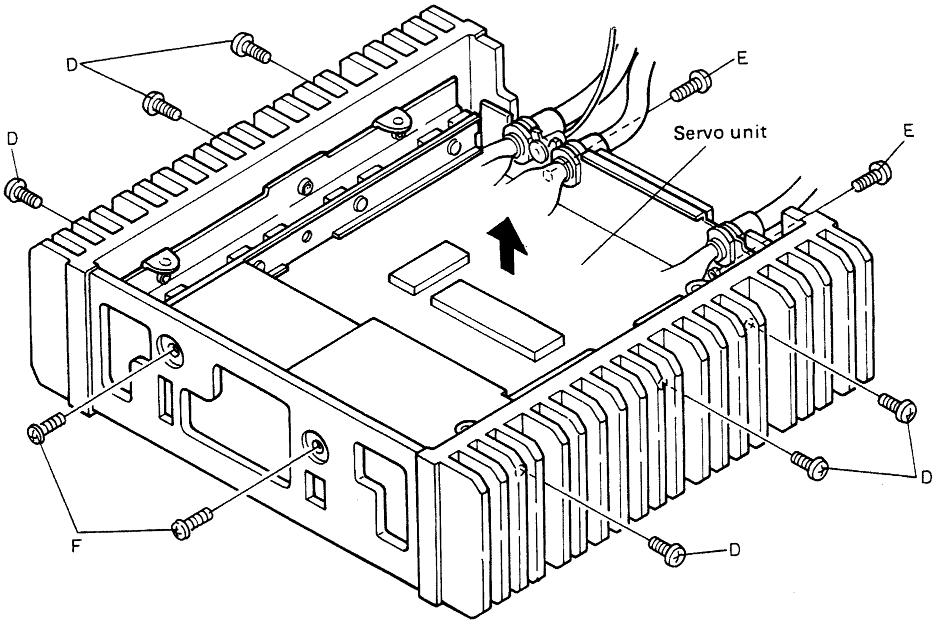

D
D
E
Servo unit
E
D
D
F

Fig. 25

8.2 PLAYER SECTION

● Removing the Case Unit

1. Remove the six screws (M3 x 4) labeled "G" which hold the case in place.

● Removing the knobs

1. Pull the knobs toward you.

● Removing the Grille Assy

1. Remove the two screws (M3 x 5) labeled "H."

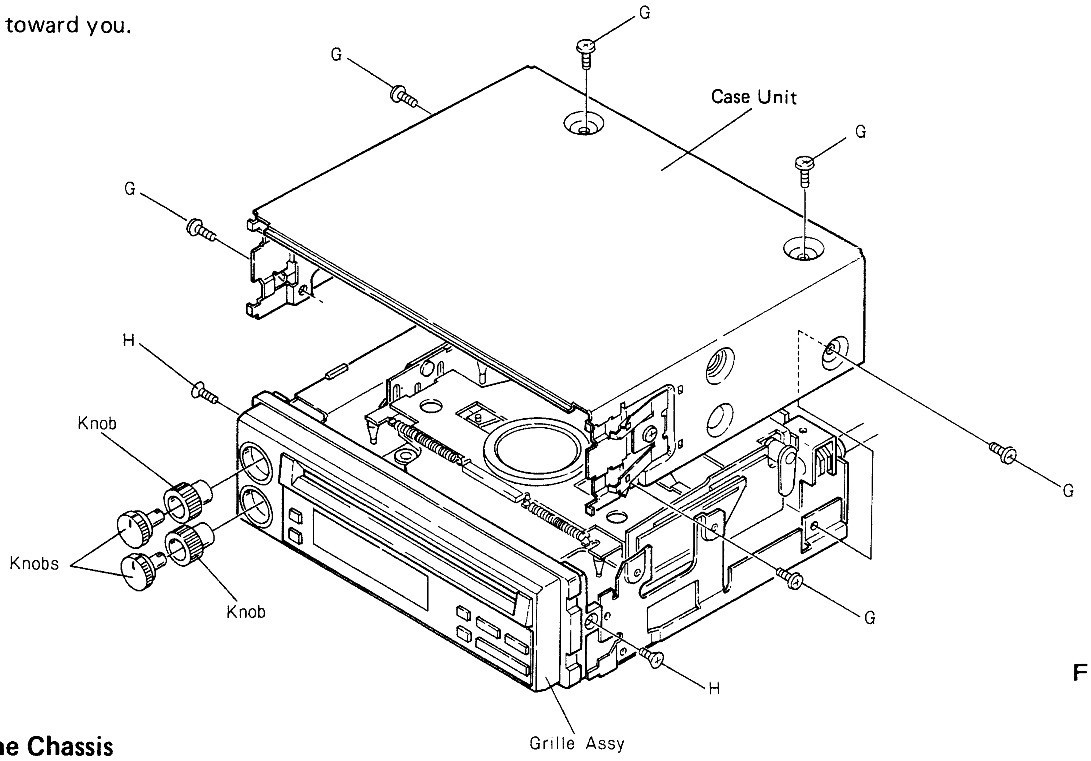

G
G
Case Unit
G
G
H
Knob
Knobs
Knob
G
G
H
Grille Assy

Fig. 26

● Removing the Chassis

1. Remove the seven screws (M2.6 x 4) labeled "K."

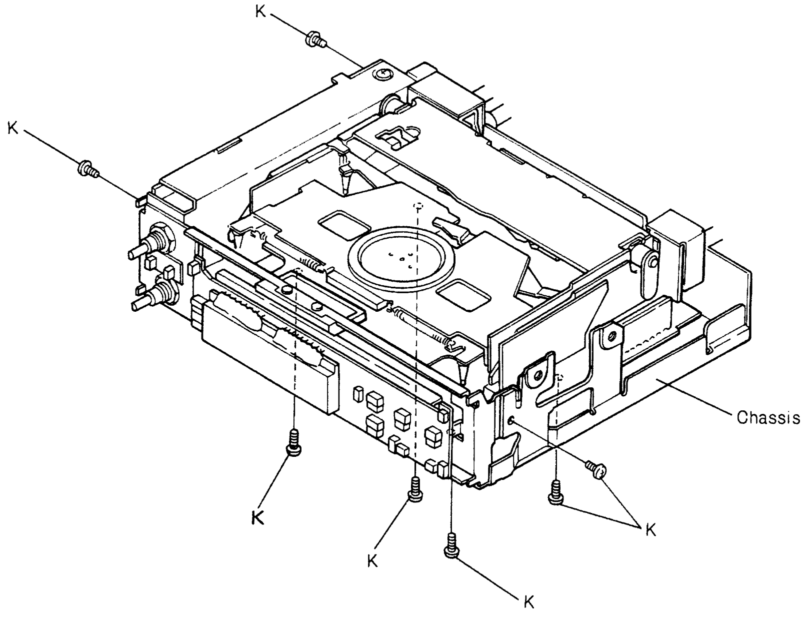

K
K
Chassis
K
K
K
K
K

Fig. 27

• Removing the Pre Amp Assy

1. Remove the screw (M2.6 x 4) labeled "L."
2. Remove the Washer and Nut.

• Removing the Display Unit

1. Remove the two screws (M2.6 X 4) labeled "M".
2. Disconnect the 3P connector.
3. Unsolder the 15 solder joints of the P. C. Board.

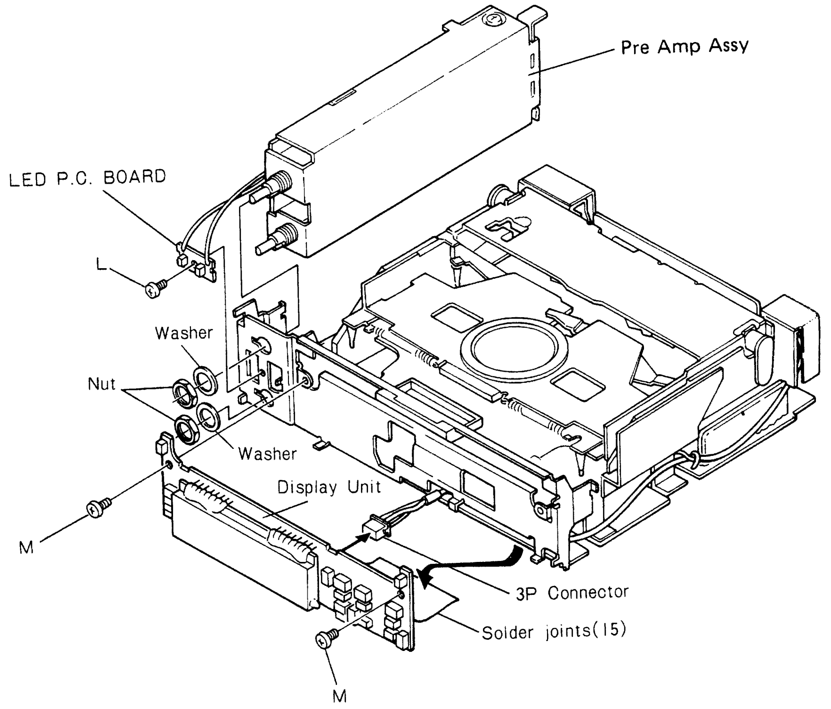

Pre Amp Assy
LED P.C. BOARD
L
Washer
Nut
Washer
Display Unit
M
3P Connector
Solder joints(15)
M

Fig. 28

• Removing the Main Unit (2/3)

1. Remove the screw (M2.6 x 4) labeled "N."
2. The unit will lift out if the catch is pulled out while lifting in the direction indicated by the arrow.

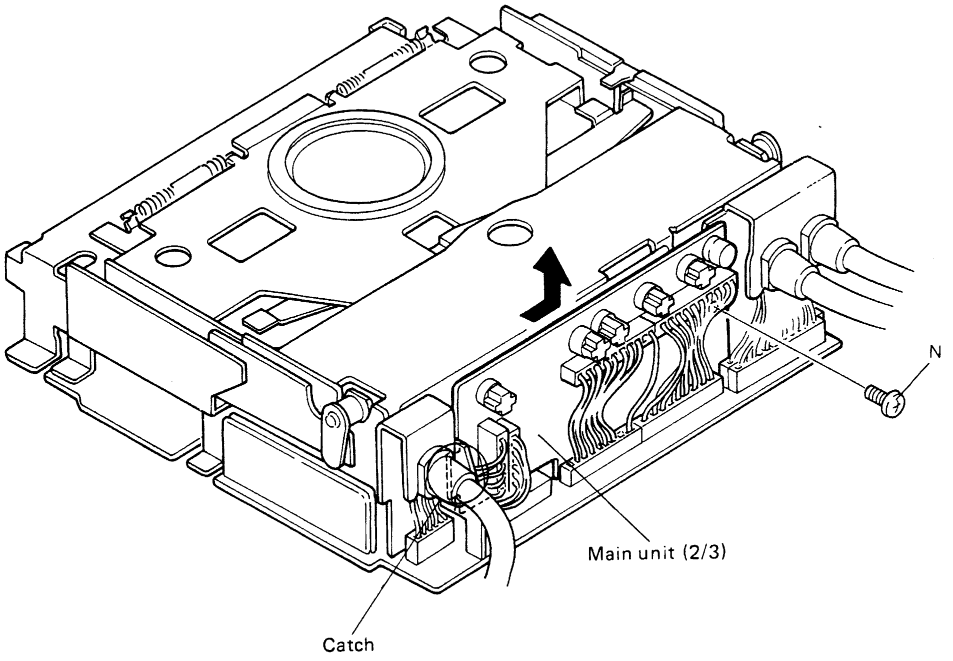

N
Main unit (2/3)
Catch

Fig. 29

Removing the Main Unit (1/3) and Mechanism Assy

1. Remove the four screws (M2.6 x 4) labeled "O."
2. The mechanism Assy may be removed by removing the connectors (4P, 6P X 2).

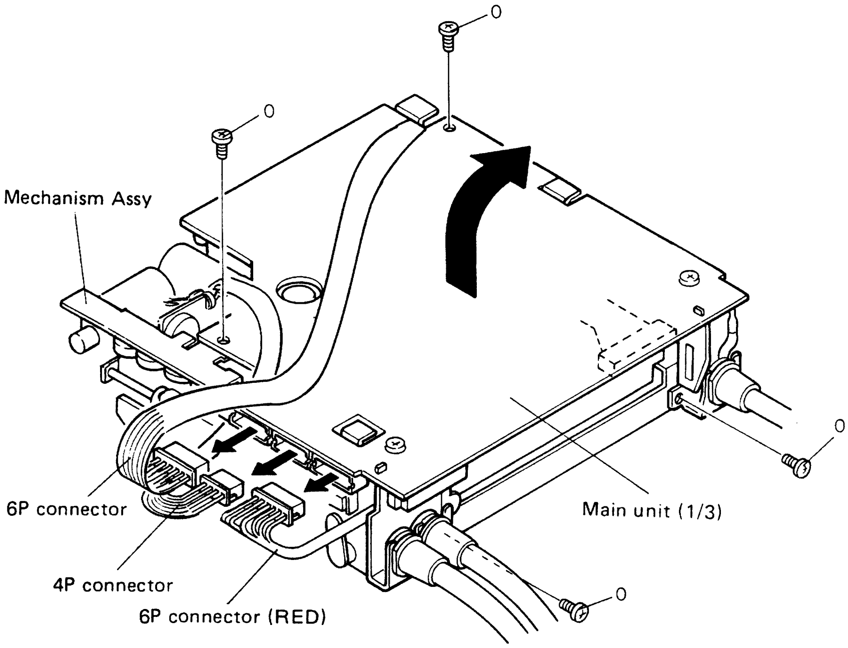

O
O
Mechanism Assy
O
6P connector
Main unit (1/3)
4P connector
O
6P connector (RED)

Fig. 30

Removing the P.C. Board

1. Insert a flathead screwdriver and turn it in the direction indicated by the arrow. The two connector clips will release, and the P.C. Board can be removed.

Note: When removing the P.C. Board from the main unit, be sure to do so after shorting the pickup (P.C. Board pattern) with a short pin as shown in Fig. 34.

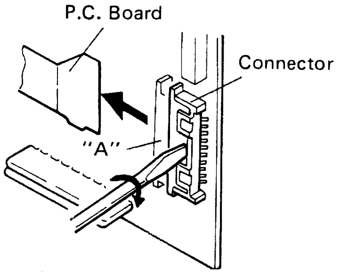

P.C. Board
Connector
"A"

Fig. 31

P.C. Board Attachment

1. Pressing the P.C. Board into place and pushing on "A" attaches the P.C. Board.

• Removing the Pickup

1. Turn the pulley in the direction indicated by the arrow until the pickup is in the removable position.
2. Remove the two screws (M3 x 4, M3 x 5) labeled "P."
3. Remove in the direction indicated by the arrow.

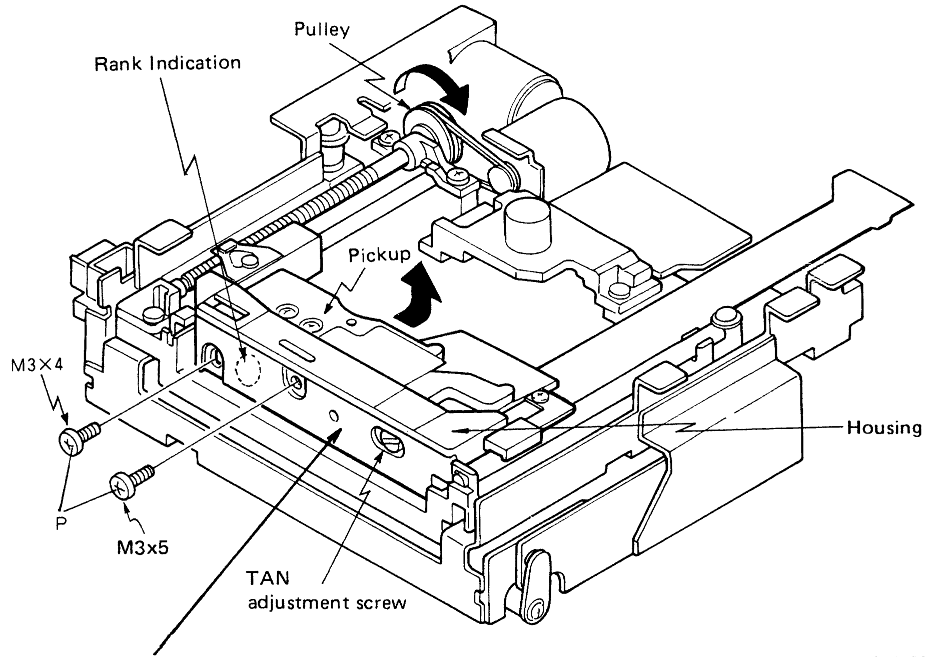

Pulley
Rank Indication
Pickup
M3X4
P
M3x5
TAN
adjustment screw
Housing

Fig. 32

Note: Be sure to attach the pickup so that it is parallel, by loosening the screw labeled "P" as shown in Fig. 33. This adjustment is the tangential direction incline adjustment shown on page 30 step 6. The adjustment is made by turning the TAN adjustment screw.

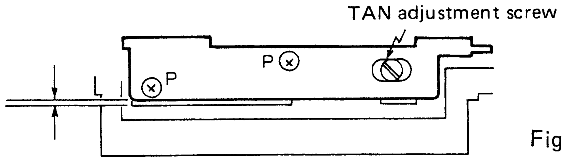

TAN adjustment screw
P
P

Fig. 33

Note: When removing the pickup be sure to short the pattern space with either a short pin or a jumper. Don't remove the short pin until after attaching the pickup and then attaching the P.C. Board (Fig. 31) to the main unit (1/3).

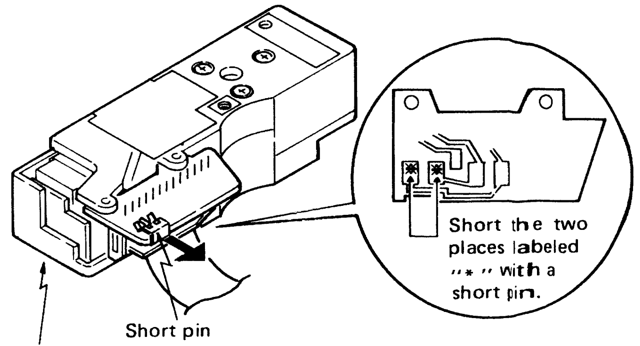

Short the two places labeled "*" with a short pin.
Short pin
Rank Indication

Fig. 34

Note:

- Mechanism unit and pickup combinations (Refer to Fig. 32 and 34 concerning ranks.)

Pickup / Mechanism unit	Rank A	Rank B	Rank C
Rank A	○	×	○
Rank B	×	○	○
Rank C	○	○	○

C: rank center

*Rank C parts are supplied as service parts.

8.3 MECHANISM UNIT

Removing the Frame

1. Remove the two screws (M2.6 x 4) labeled "R."

Removing the Plate

1. Remove the screw (M2 x 4) labeled "S," and the arm units "A" and "B."
2. Remove the screw (M2.6 x 3) labeled "T," the bracket, and the lever.
3. Remove the two screws (M2.6 x 4) labeled "U" and the lever unit.
4. The plate unit can be removed by pulling in the direction indicated by the arrow.

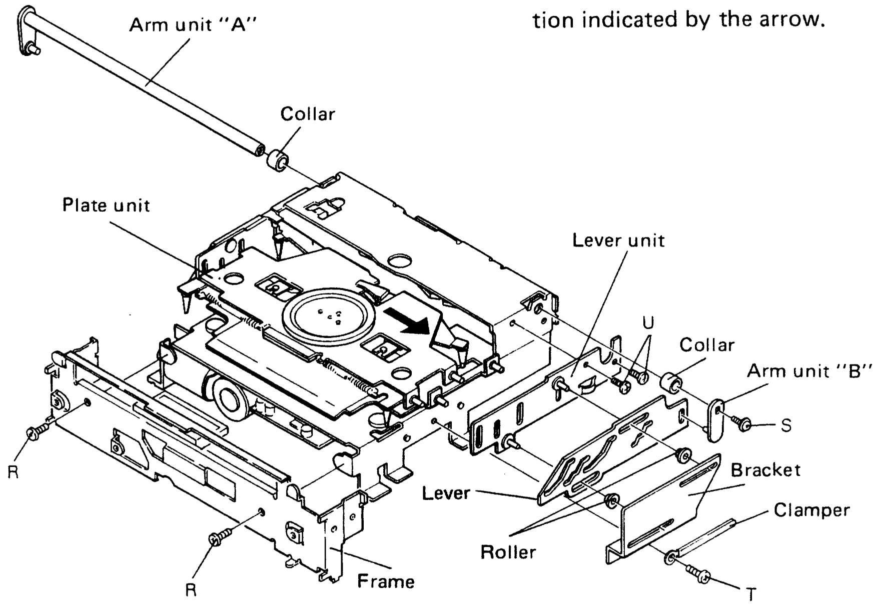

Arm unit "A"
Collar
Plate unit
Lever unit
U
Collar
Arm unit "B"
S
Bracket
Clamper
Lever
Roller
R
R
Frame
T

Fig. 35

Removing the Plate Unit

1. Remove the two screws (M2 x 3) labeled "V" and the screw (M2.6 x 4) labeled "W."
2. It can be removed by pulling in the direction indicated by the arrow.

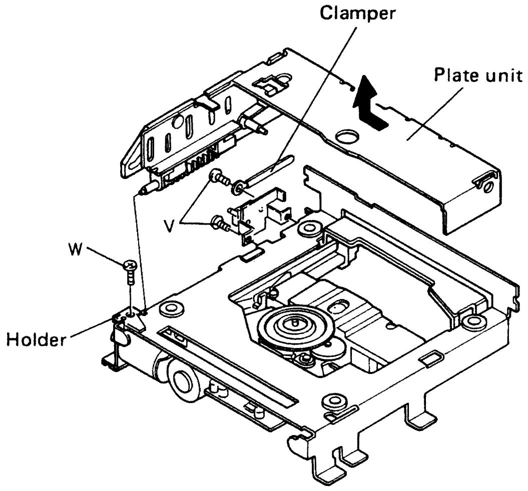

Clamper
Plate unit
V
W
Holder

Fig. 36

Removing the Spindle Motor

1. Remove the two screws (M2.6 x 6) labeled "X."
2. Slide the pulley in the direction indicated by the arrow and remove the spindle.

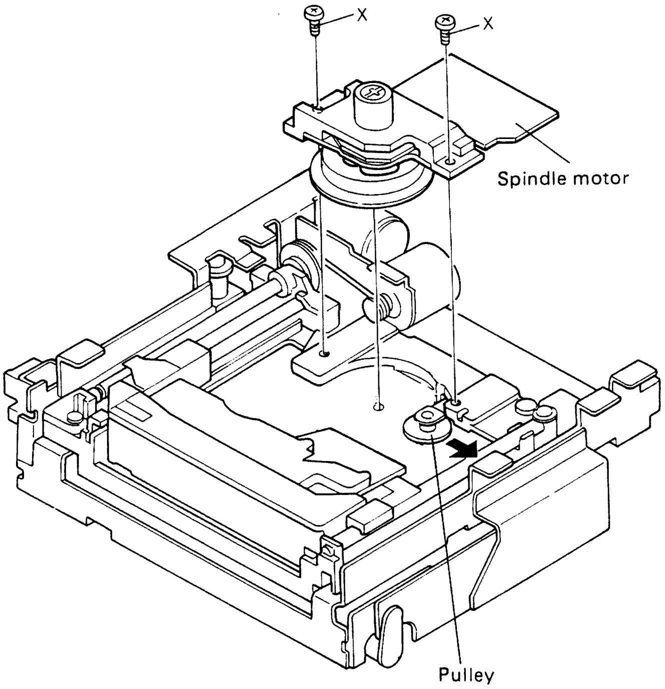

X
X
Spindle motor
Pulley

Fig. 37

NOTE: Take care not to let the spindle motor fly wheel shaft become scratched or dirty.

Removing the Carriage Motor

1. Remove the two screws (M2.6 x 4) labeled "Y."
2. Remove the belt.

NOTE:
Before attaching the belt, make sure that it is not soiled with grease and not twisted.

Removing the Loading Motor

1. Remove the screw (M2.3 x 4) labeled "Z."

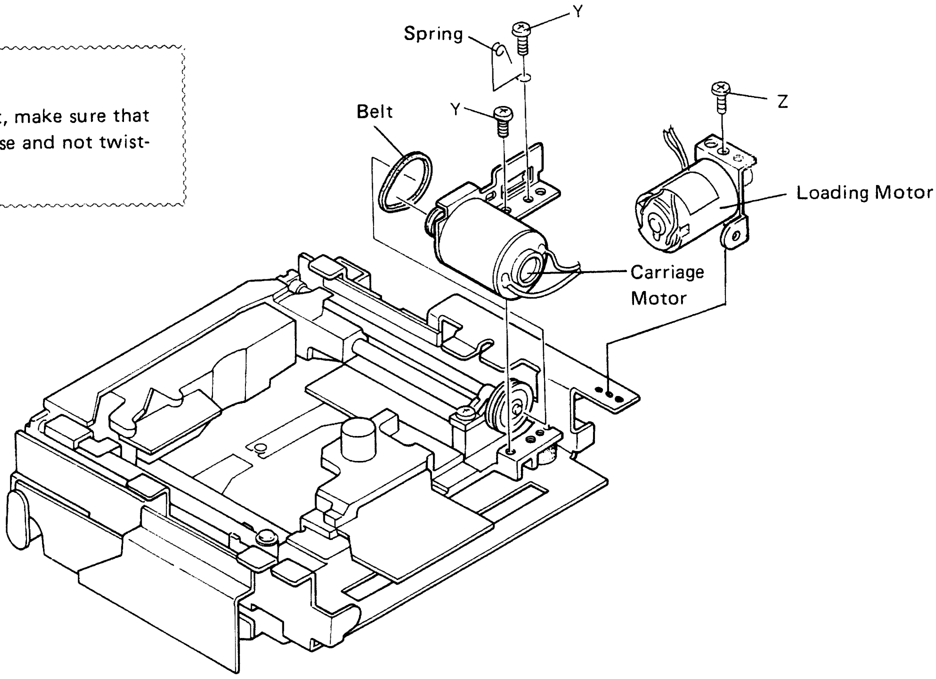
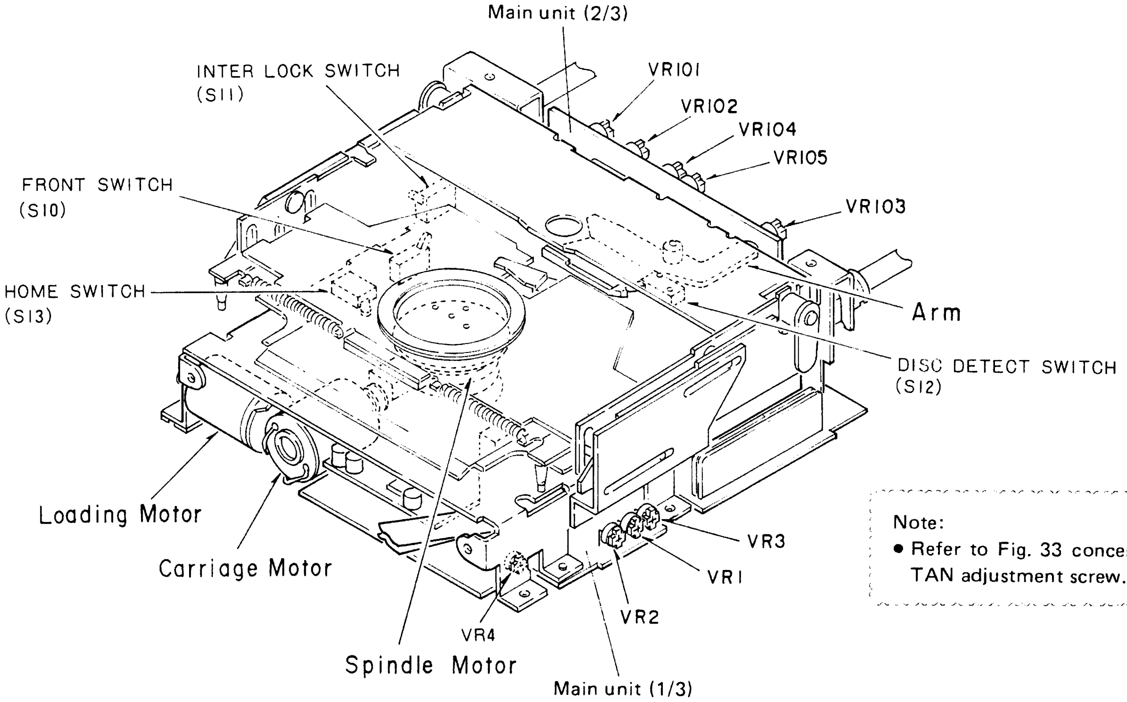

Spring
Y
Belt
Y
Z
Loading Motor
Carriage Motor

Fig. 38

9. ADJUSTMENT

• Adjustment Points (Player Section)


Main unit (2/3)
INTER LOCK SWITCH (S11)
VR101
VR102
VR104
VR105
VR103
FRONT SWITCH (S10)
HOME SWITCH (S13)
Arm
DISC DETECT SWITCH (S12)
Loading Motor
Carriage Motor
VR3
VR1
VR2
VR4
Spindle Motor
Main unit (1/3)

Note:
- Refer to Fig. 33 concerning the TAN adjustment screw.

Fig. 39

• Main Unit (1/3) Pattern Diagram (Test Points)

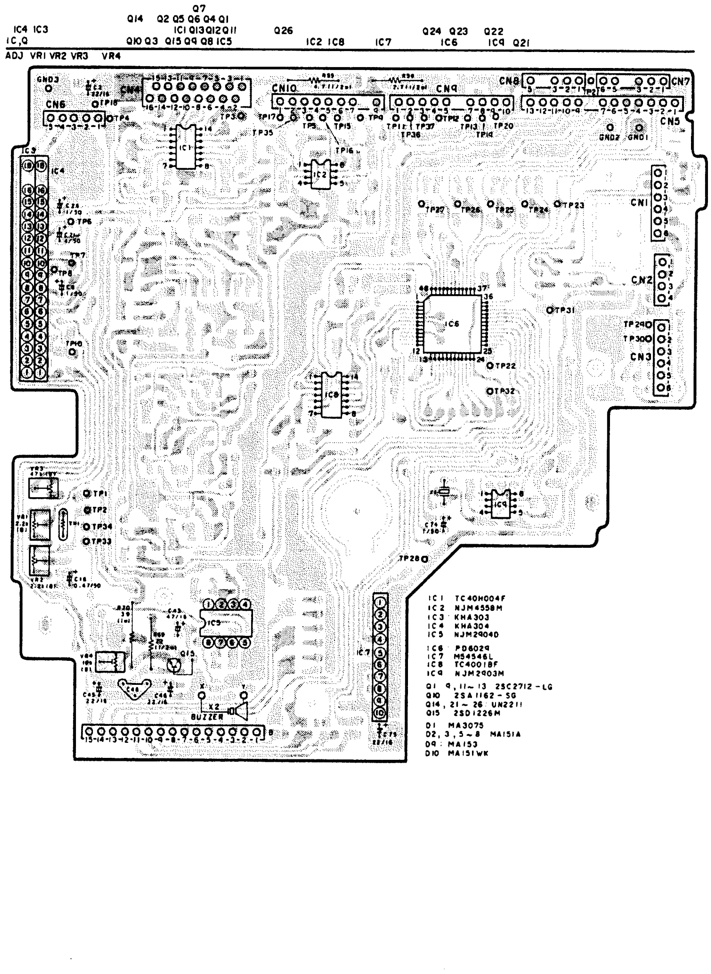

Q7
Q14 Q2 Q5 Q6 Q4 Q1
IC4 IC3 IC1 Q13 Q12 Q11 Q26 Q24 Q23 Q22
IC,Q Q10 Q3 Q15 Q9 Q8 IC5 IC2 IC8 IC7 IC6 IC9 Q21
ADJ VR1 VR2 VR3 VR4
GND3
CN6
CN4
CN10
CN9
CN8
CN7
CN5
CN1
CN2
CN3
GND2 GND1
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
TP16
TP17
TP18
TP20
TP22
TP23
TP24
TP25
TP26
TP27
TP28
TP30
TP31
TP32
TP33
TP34
TP35
TP36
TP37
IC1
IC2
IC3
IC4
IC5
IC6
IC7
IC8
IC9
BUZZER
IC1 TC40H004F
IC2 NJM4558M
IC3 KHA303
IC4 KHA304
IC5 NJM2904D
IC6 PD6029
IC7 M54546L
IC8 TC40018F
IC9 NJM2903M
Q1 9, 11~13 2SC2712-LG
Q10 2SA1162-SG
Q14, 21~26 UN2211
Q15 2SD1226M
D1 MA3075
D2, 3, 5~8 MA151A
D9 MA153
D10 MA151WK

Fig. 40

- **Adjustment Points (Hideaway Unit Section)**

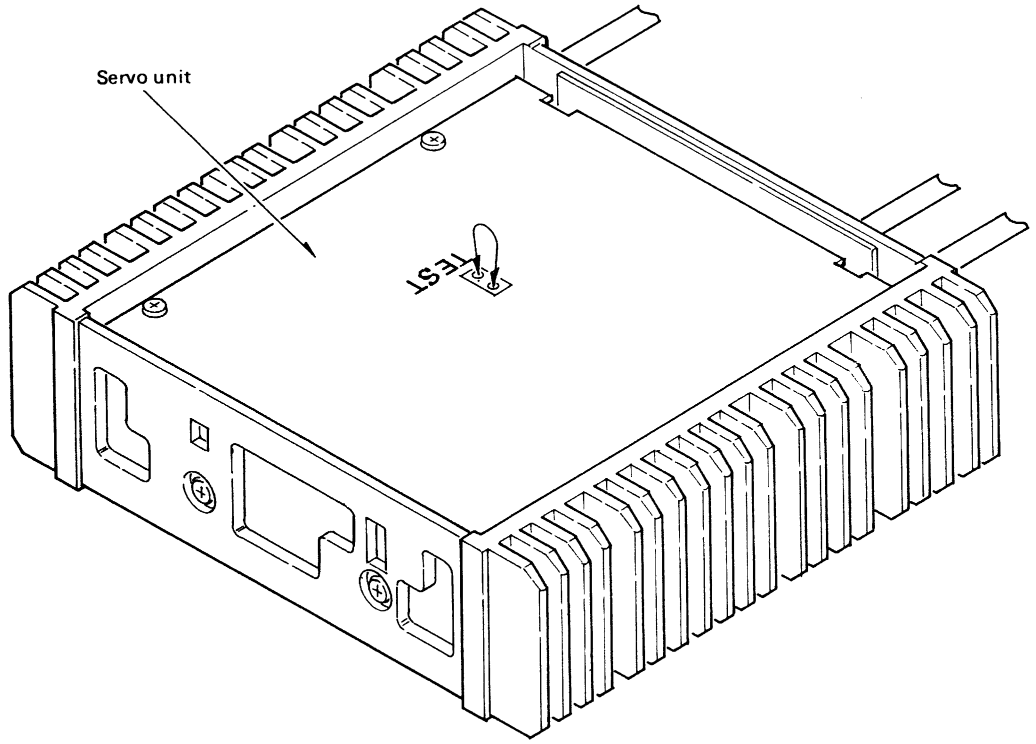

Servo unit
TEST

Fig. 41

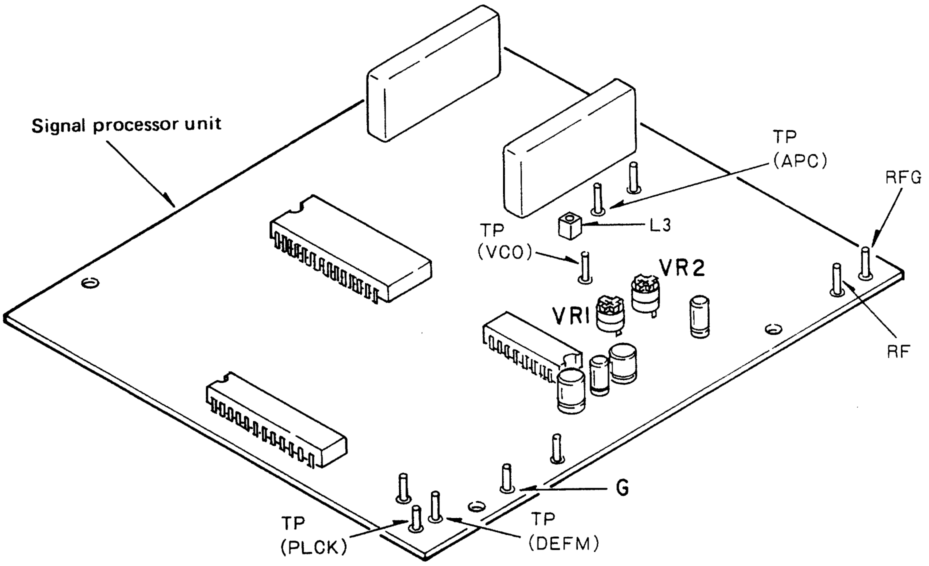
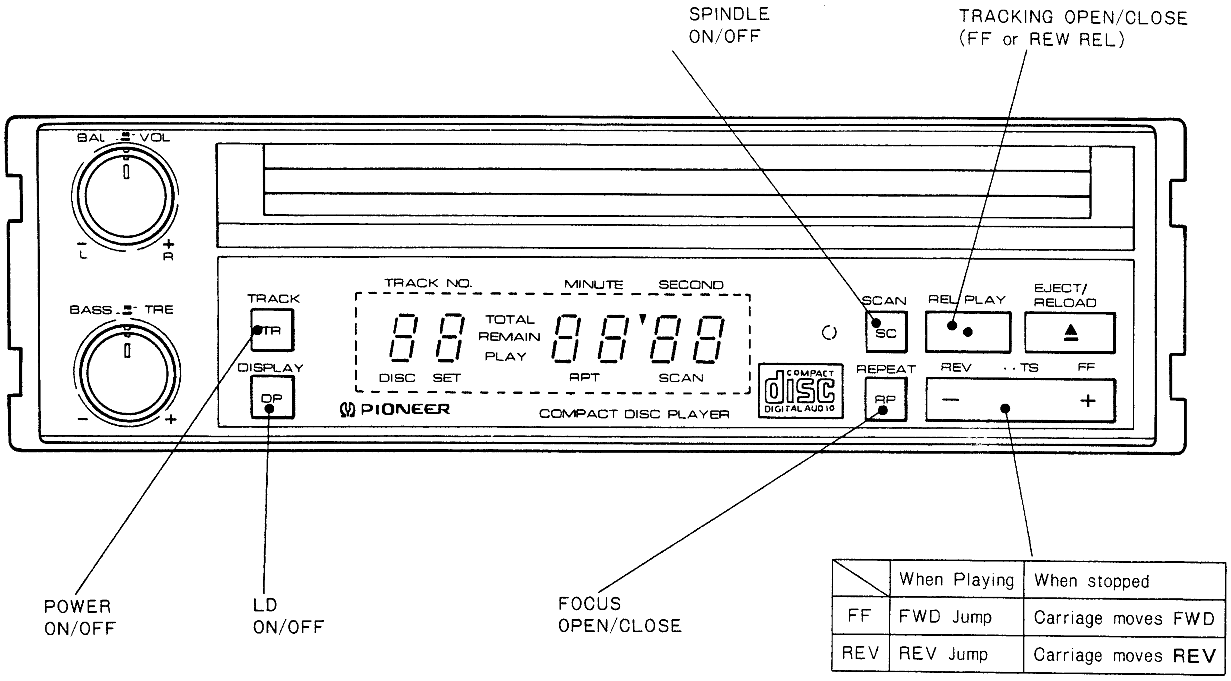

Signal processor unit
TP (APC)
RFG
L3
TP (VCO)
VR2
VR1
RF
G
TP (PLCK)
TP (DEFM)

Fig. 42

Test Mode Key Functions


SPINDLE ON/OFF
TRACKING OPEN/CLOSE (FF or REW REL)
BAL VOL
L
R
BASS TRE
TRACK
TR
DISPLAY
DP
TRACK NO.
MINUTE
SECOND
TOTAL
REMAIN
PLAY
DISC
SET
RPT
SCAN
PIONEER
COMPACT DISC PLAYER
COMPACT disc DIGITAL AUDIO
SCAN
SC
REL/PLAY
EJECT/ RELOAD
REPEAT
RP
REV
TS
FF
POWER ON/OFF
LD ON/OFF
FOCUS OPEN/CLOSE

	When Playing	When stopped
FF	FWD Jump	Carriage moves FWD
REV	REV Jump	Carriage moves REV

Fig. 43

CD Player Test Mode Switch Functions

Note: In the test mode, the track number and time display both reset to zero.

(00 TRACK NO. 00 MINUTE 00 SECOND)

No.	Switch name		Function	Display	Operation description	Comments
1	TR TRACK		POWER: ON/OFF	ON: PLAY	Makes the PD3036 pin 18 ($\overline{\text{power}}$) "L,"and starts the DC-DC converter.	It won't operate if NO.1 (TR) is not on.
2	DP DISPLAY		LD POWER : ON/OFF	ON : SET	Makes the PD6029 pin 1 ($\overline{\text{LD}}$) "L," and fires the laser diode.	It won't operate if NO.1 (TR) is not on.
3	SC SCAN		Spindle motor: ON/OFF	ON : DISC	Makes the PD3036 pin 20 (P/$\overline{\text{S}}$) "H," and turns the spindle motor.	It won't operate if NO.1 (TR) is not on.
4	RP REPEAT		Focus servo: OPEN/CLOSE	CLOSE : ART	Makes the PD8010 pin 13 ($\overline{\text{PUSH}}$) "H," and closes the focus servo loop.	
5	REL/PLAY		Tracking servo: OPEN/CLOSE	CLOSE : SCAN	Makes the PD8010 pin 17 (T-o/$\overline{\text{c}}$) "L," and closes the tracking servo loop.	Pushing this button once turns buttons one to four on changing the functions of the buttons. This stage persists until either the power is turned off or the clear button is pushed.
6	FF (+)	While playing	Forward jump	———	Outputs pulses to PD8010 pins 20 ($\overline{\text{J}}$-), 19 ($\overline{\text{J}}$+) and 18 (T-AS) [causing a forward jump].	Normally playing (test mode).
		While stopped.	Drives the carriage motor	———	Makes the PD8010 pin 15 ($\overline{\text{F}}$/R) "L," and outputs a pulse to pin 16 (R-O/C) driving the carriage.	It won't operate if NO.1 (TR) is not on.
7	REV (–)	While playing	Reverse jump	———	Outputs pulses to PD8010 pins 20 ($\overline{\text{J}}$-) 19 ($\overline{\text{J}}$+) and 18 (T-AS)[causing a reverse jump].	Normally playing (test mode)
		While stopped.	Drives the carriage motor backward.	———	Makes the PD8010 pin 15 ($\overline{\text{F}}$/R) "H," and outputs a pulse to pin 16 (R-O/$\overline{\text{C}}$) driving the carriage.	It won't operate if NO.1 (TR) is not on.

Step No.	Oscilloscope range		Test point	Adjustment point	Item to verify/ adjustment method	Adjustment steps (player section)
	X	Y				

Instruments used in adjustments and repairs

- Two-channel oscilloscope with delayed sweep
- Light power meter
- Test disc (YEDS-7)

- DC power supply (15 A or more)
- FTG Adaptor JIG (GGF-044)
- FTG Adjustment JIG (GGV-096)
- LPF-JIG (GGF-045)

Caution

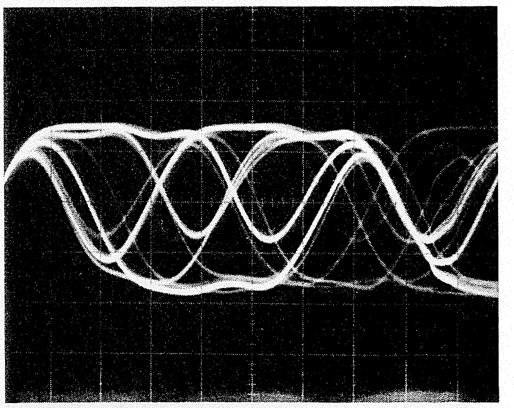
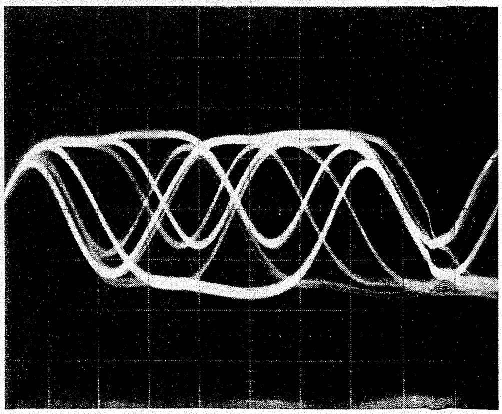
- It is assumed that the oscilloscope has a 10:1 probe.
- The waveform pictures were taken using an oscilloscope with a 100 MHz band.
- Don't look into the object lens when the laser is on.
- Perform steps five through fifteen with the test disc in place.

Preparations

- Remove the upper and lower cases from the player section. When adjusting the tangential direction (step six) however, remove the main unit (2/3) first.
- Remove the upper and lower cases of the hideaway unit section.
- Be sure to short the pattern inside the TEST window of the servo unit of the hideaway unit section, (switching to test mode) before turning on the power supply.
- Connect the player section and hideaway unit section.

Note:
Remove the servo unit pattern short from the hideaway unit section after making adjustments.

Step No.	Oscilloscope range		Test point	Adjustment point	Item to verify/ adjustment method	Adjustment steps (player section)
	X	Y				
1	20mV/div	1ms/div	TP35	—	0 ± 50mV	**Focus return voltage check** ● Push the arm and while turning off the DISC DETECT SW (S12), press the EJECT/RELOAD button to initiate loading. Use a flathead screwdriver to push the arm, being careful that it doesn't get caught. ● Push the TRACK button and make sure that the Focus return voltage is within specifications.
2	20mV/div	1ms/div	TP36	VR103	0 ± 5mV	**Tracking return voltage check and adjustment** ● As in step one, make sure that the tracking voltage is within specifications. If it isn't, adjust it using VR103 until it comes within specifications.
3	—	—	—	—	—	**Actuator operation check.** ● Starting with step two, push the FF button and move the pickup toward the outside edge of the disc until it is in a place where it can be checked. ● Push the REPEAT button and make sure that the pickup object lens moves up and down. Note: Check this for two seconds or less, and then push the REPEAT button again and stop the movement of the object lens. ● Press the EJECT/RELOAD button to eject the disc.
4	—	—	—	VR4	0.25 ± 0.01mW	**LD power check and adjustment** ● While pushing the INTER LOCK SW (S11), push the FF button and move the pickup until the power sensor enters. ● Place the power sensor on top of the pickup object lens. ● Push the DISPLAY button, turn on the LD and check the emitting power. If it is not within specifications, quickly adjust it using VR4. ● After adjustment, push the DISPLAY button again and turn off the LD. Note: When replacing the pickup, set VR4 to the minimum (turn completely to the left) and then begin adjustment. Also, do this with the INTER LOCK SW (S11) held down.

Step No.	Oscilloscope range		Test point	Adjustment point	Item to verify/ adjustment method	Adjustment steps (player section)
	X	Y				
5	50mV/div	0.5μs/div	TP4 (RF, RFG) Signal processor unit	VR104	Maximum RF level	**Focus offset coarse adjustment** • While pushing the INTER LOCK SW (S11), push the TRACK button and then the REV button and move the pickup toward the center of the disc. • Insert a test disc and load it with the EJECT/RELOAD buttons. • Turn on the LD with the DISPLAY button, and push the SCAN, REPEAT, and REL/PLAY buttons to make it play. • Push the FF button and go to the 23rd selection (approximately 23 minutes). The jump operation can be canceled with the REL/PLAY button. • Adjust the VR104 so that the RF level is at its maximum. Note: Steps five through fifteen take place with the test disc inserted.
6	50mV/div	0.5μs/div	TP4 (RF, RFG) Signal processor Unit	TAN adjustment screw	See waveforms	**Tangential direction incline adjustment** • Play selection 23 (approximately 23 minutes). • Adjust the tangential adjustment screw until the RF waveform peaks flatten out. NG  Fig. 45 NG  Fig. 46

OK

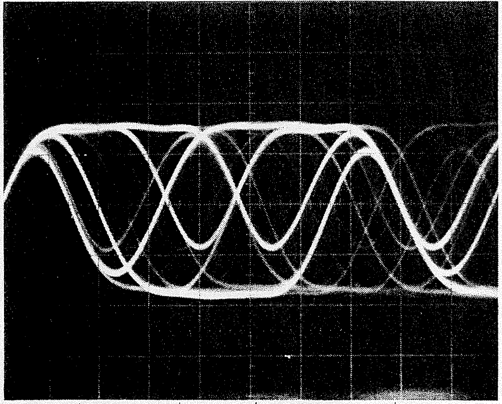
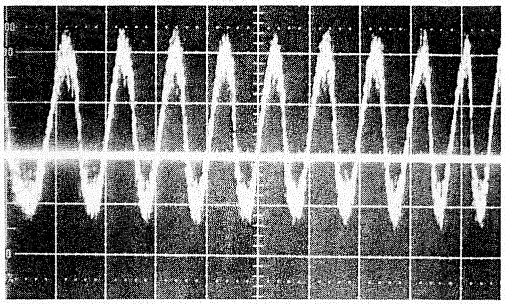
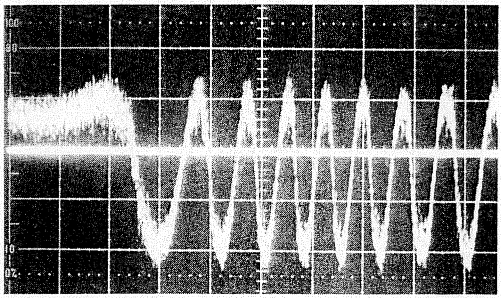
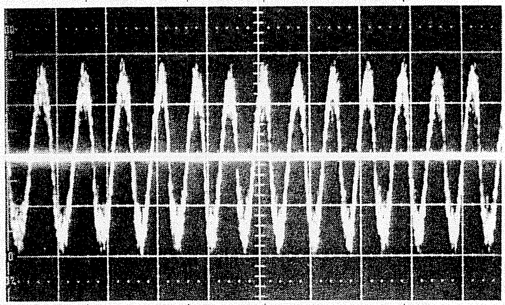
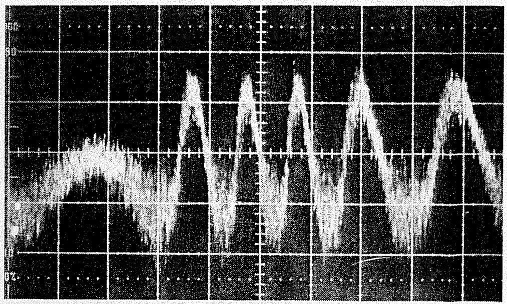
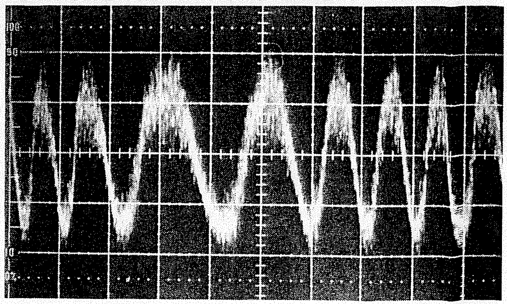
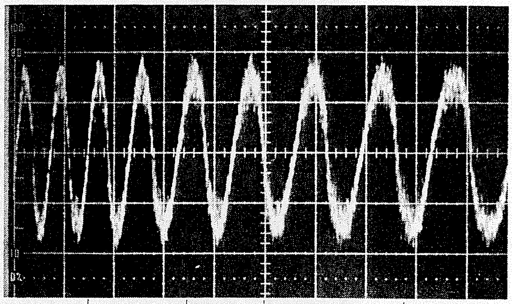
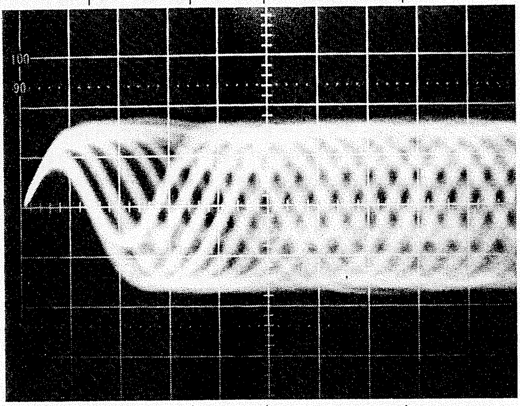
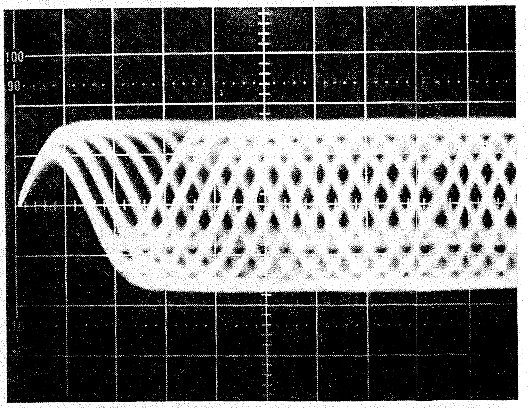


Fig. 44

Step No.	Oscilloscope range		Test point	Adjustment point	Item to verify/ adjustment method	Adjustment steps (player section)
	X	Y				
7	0.2V/div	1μs/div	TP37	VR3	See waveforms	**Tracking error offset adjustment** - Play selection 14 (approximately 14 minutes). - With the REL/PLAY button pushed and the tracking servo open, adjust VR3 so that the waveform center is 0 volts. NG  Fig. 49 NG  Fig. 50
OK	 Fig. 47					
8	0.2V/div	1μs/div	TP37	————	See waveforms	**Radial direction incline check** - The TE waveform positive and negative noise component should be less than or equal to half of the peak value of either the positive or negative side. (Not including the noise.) Check both the center and outside edge of the disc. NG  Fig. 51 NG  Fig. 52
OK	 Fig. 48					

Step No.	Oscilloscope range		Test point	Adjustment point	Item to verify/ adjustment method	Adjustment steps (player section)
	X	Y				
9	10mV/div	1ms/div	TP35	———	Innermost track – 200 mV ±450 mV Outermost track. –200 mV ±560 mV Difference between innermost and outermost tracks should be within 90 mV.	**Spindle radial direction incline check** • Push the REV button and play the innermost track. • Make sure that the focus return DC voltage is within specifications. • Push the FF button and play the outermost track. • Make sure that the focus return DC voltage is within specifications. • Make sure that the DC voltage difference between the innermost and outermost tracks is within specifications. NOTE: Read the voltage of the waveform center by converting it into a DC value.
10	50mV/div	0.5μs/div	TP4 (RF, RFG) Signal processor unit	VR104	See waveforms	**Fine adjustment of focus offset** • Play selection 14 (approximately 14 minutes). • Adjust VR104 so that the RF output eye pattern is optimal (minimum jitter component). (minimum jitter component with maximum RF)
NG					Fig. 53	OK  Fig. 54
11	0.2V/div	1ms/div	TP37	VR1	5 ± 0.5Vp-p	**Tracking error level adjustment** • Play selection 14 (approximately 14 minutes). • Push the REL/PLAY button and open the tracking servo. Then adjust VR1 until the tracking error level is within specifications. However, the level should be read at the noise center. Note: If the tracking error offset adjustment has been shifted, then begin adjustment with step seven.
12	50mV/div	0.5μs/div	TP4 (RF, RFG) Signal Processor unit	VR2	1.5 ± 0.2V	**RF output level adjustment** • Play selection 14 (approximately 14 minutes). • Adjust VR2 until the RF output is within specifications.

Step No.	Oscilloscope range		Test point	Adjustment point	Item to verify adjustment method	Adjustment steps (player section)
	X	Y				
13	———	———	TP15 TP17	VR105		**Focus servo gain adjustment** (a) Turn the selector switch of the jig to 1. (b) Use search to locate track #14. (c) Connect Orange wire to TP15, Brown wire to TP17, and Black wire to TP18 (GND). (d) Adjust VR105 to turn J-LED on.
14	———	———	TP12 TP13	VR101		**Tracking servo gain adjustment** (a) Turn the selector switch of the jig to 2. (b) Use search to locate track #14. (c) Connect Yellow wire to TP12, Red wire to TP13, and Black wire to TP18 (GND). (d) Adjust VR101 to turn J-LED on.

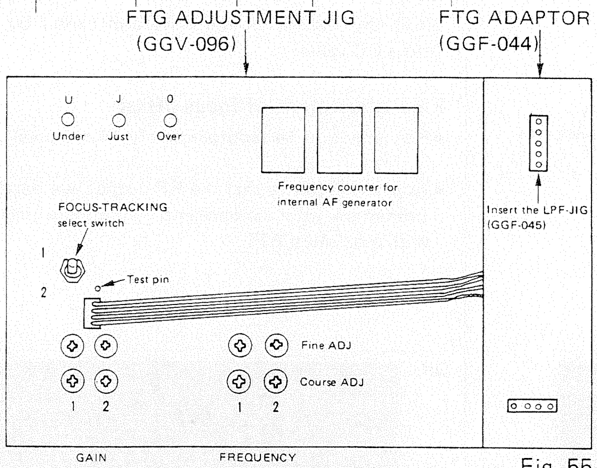

FTG ADJUSTMENT JIG (GGV-096)
FTG ADAPTOR JIG (GGF-044)
U
J
O
Under
Just
Over
Frequency counter for internal AF generator
FOCUS-TRACKING select switch
1
2
Test pin
Insert the LPF-JIG (GGF-045)
Fine ADJ
Course ADJ
1
2
1
2
GAIN
FREQUENCY

Fig. 55

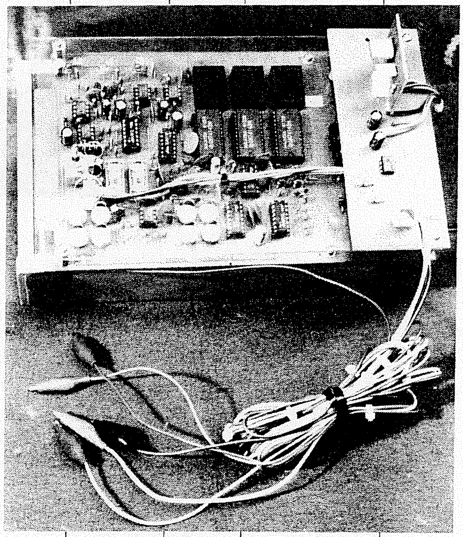
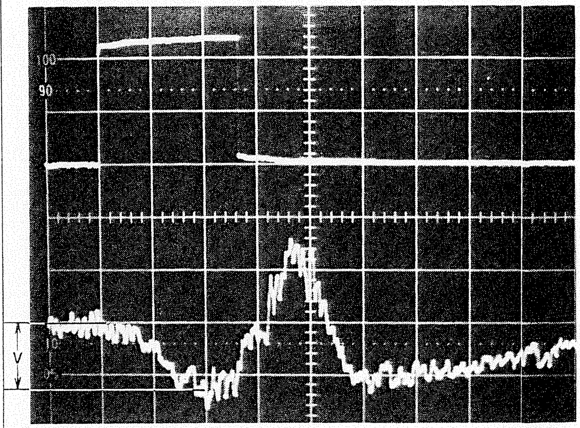
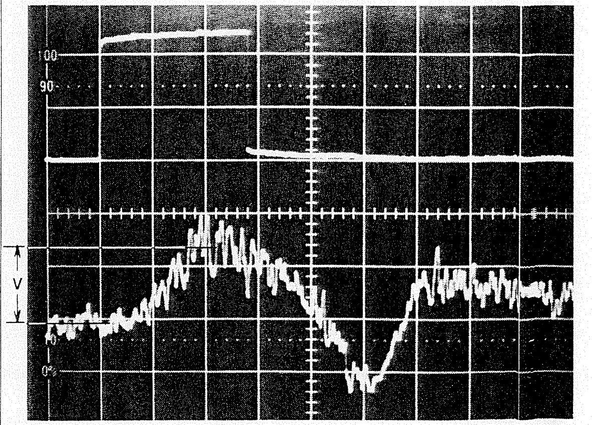
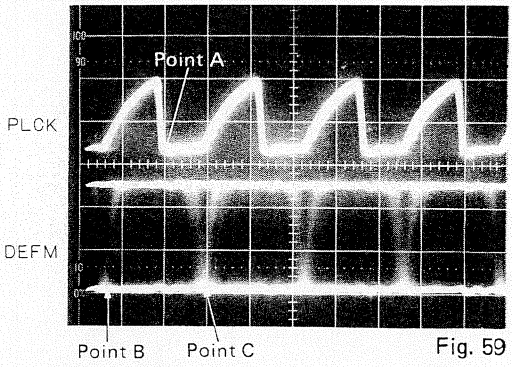
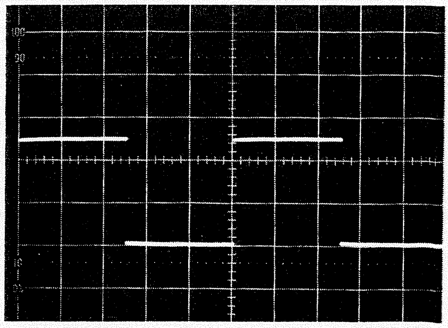


Fig. 56

- Initial setting the FTG ADJUSTMENT JIG

(a) Insert the connector of the LPF-JIG (GGF-045) for CDX-P1 into the connector on the FTG ADJUSTMENT JIG.
(b) Turn the power switch on.
(c) Turn the FOCUS-TRACKING selector switch on the jig to 1. Set the oscillating frequency of the internal oscillator at 600 Hz with the frequency potentiometer-1. The oscillating frequency is displayed on the 7-segment LEDs. First, adjust the frequency roughly with the lower side potentiometer, then adjust it finely with the upper side potentiometer.
(d) Connect the probe of oscilloscope at the TEST PIN located at the right side of the selector switch. Adjust the GAIN potentiometer-1 so that the peak to peak voltage of the waveform at the TEST PIN is 140mV.
(e) Turn the selector switch on the jig to 2. In the same procedure above, adjust FREQ potentiometer-2 so that the oscillating frequency of the internal oscillator is 1.5KHz.
(f) In the same procedure above, adjust the GAIN potentiometer-2 so that the peak to peak voltage of the waveform at the TEST PIN is 140mV.

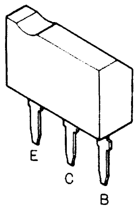
Step No.	Oscilloscope range		Test point	Adjustment point	Item to verify/ adjustment method	Adjustment steps (player section)
	X	Y				
15	$\boxed{CH1}$ 0.5V/div	0.1ms/div	TP11	VR102	250 ± 50μs	**Jump gain adjustment** ● Play selection 10 (approximately 10 minutes); then press the $\boxed{FF}$ button (forward jump). ● Adjust VR102 until the $\overline{\text{T-AS}}$ signal (TP11) "H" level space is within specifications. ● Observe the TE waveform and make sure that the overshoot quantity after a jump is less than or equal to half the jump peak value. If it isn't, Adjust VR102 until it is within specifications. Make sure that the $\overline{\text{T-AS}}$ signal "H" level space is within specifications at this time.  Fig. 57 ● Play selection 20 (approximately 20 minutes); then press the $\boxed{REW}$ button (reverse jump). ● Make sure that the "H" level port of the $\overline{\text{T-AS}}$ signal is within specifications. ● Make sure that the TE waveform overshoot quantity after the jump is also within specifications.  Fig. 58
	$\boxed{CH2}$ 0.1V/div	0.5ms/div	TP37	VR102		

Step No.	Oscilloscope range		Test point	Adjustment point	Item to verify/ adjustment method	Adjustment steps (Hideaway unit section)
	X	Y				
						Instruments used in adjustments and repairs ● Two-channel oscilloscope with delayed sweep ● Test disc (YEDS-7 or demonstrations disc) ● DC power supply (15 A or more) **Caution** ● It is assumed that the oscilloscope has a 10 : 1 probe. **Preparations** ● For the hideaway unit section, set up the signal processor by removing the four screws, avoiding short circuits. ● Connect the player section and the hideaway unit section.
1	0.1V/div	1ms/div	VCO	L3	4.3V	**VCO adjustment** ● Insert the disc and set to play. ● Adjust L3 until the DC voltage is within specifications
2	CH1 0.2V/div CH2 0.2V/div	0.1μs/div 0.1μs/div	DEFM PLCK	VR1		**PLL phase adjustment** ● Insert the disc and set to play. ● Connect TP (DEFM) to channel one and TP (PLCK) to channel two (set the trigger with PLCK). ● Align the PLCK trailing edge (point A) to the DEFM jitter center (between points B and C).  Fig. 59
3	0.2V/div	50μs/div	APC	VR2	Duty ratio 50%	**SPDL offset adjustment** ● Insert the disc and set to play. ● Adjust VR2 so that the signal at the APC (automatic phase control) has a duty ratio of 50%.  Fig. 60

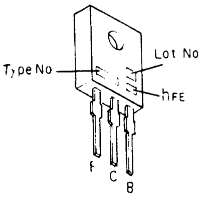
10. ICs AND TRANSISTORS INFORMATION

*IC's marked by * are MOS type.*
Be careful in handling them because they are very liable to be damaged by electrostatic induction.

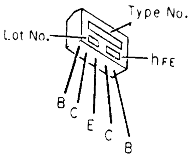
2SD1226M



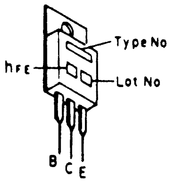
2SC1847
2SA886


Type No
Lot No
hFE
E
C
B

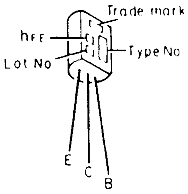
2SA798


Type No.
Lot No.
hFE
B
C
E
C
B

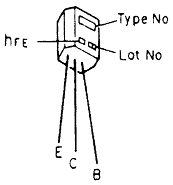
2SC2654


Type No
hFE
Lot No
B
C
E

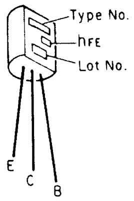
2SA683


Trade mark
hFE
Lot No
Type No
E
C
B

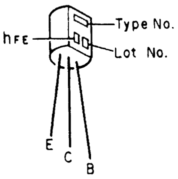
2SC2458
2SA1048
2SA1048L
2SA933SLN


Type No
hFE
Lot No
E
C
B

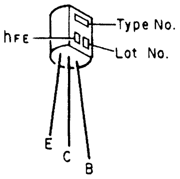
2SB647
2SD468

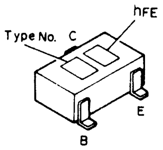

Type No.
hFE
Lot No.
E
C
B

2SC1740S


Type No.
hFE
Lot No.
E
C
B

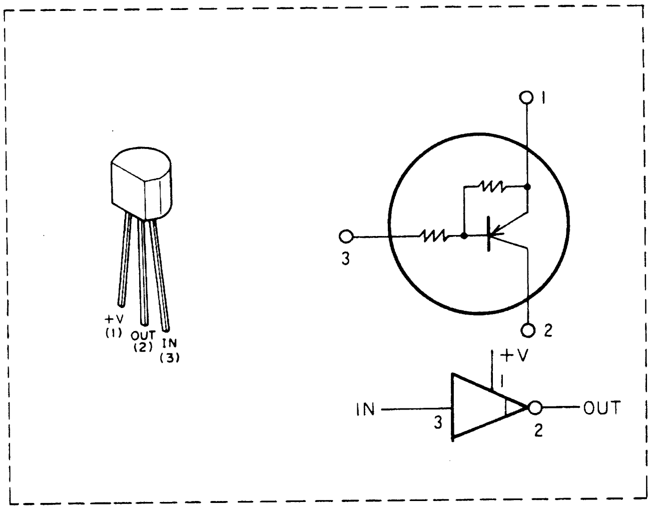
2SC1815
2SA1015


Type No.
hFE
Lot No.
E
C
B

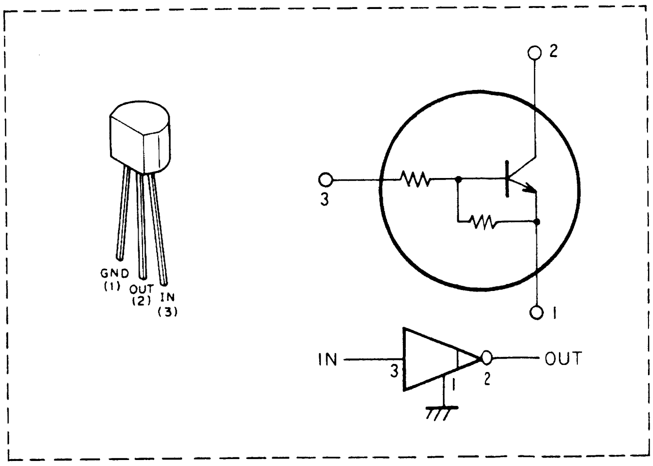
Parts No.	Indication(Type No., hFE)
2SC2712-LG	LG 
2SC2712-LL	LL
2SA1162-SG	SG
2SA1162-SY	SY

hFE
Type No.
C
E
B

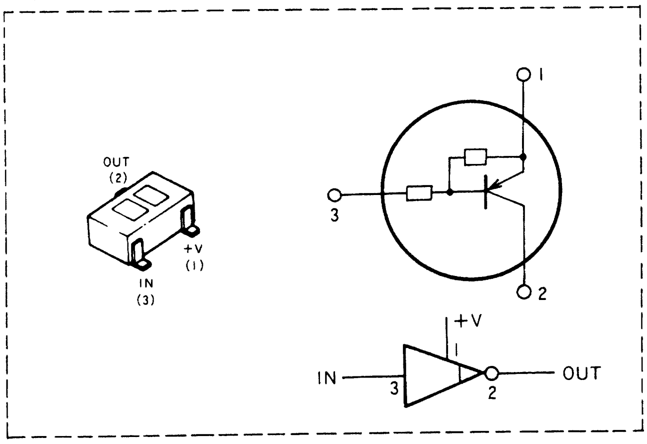
DTA124ES


+V
(1)
OUT
(2)
IN
(3)
1
3
2
+V
1
IN
3
2
OUT

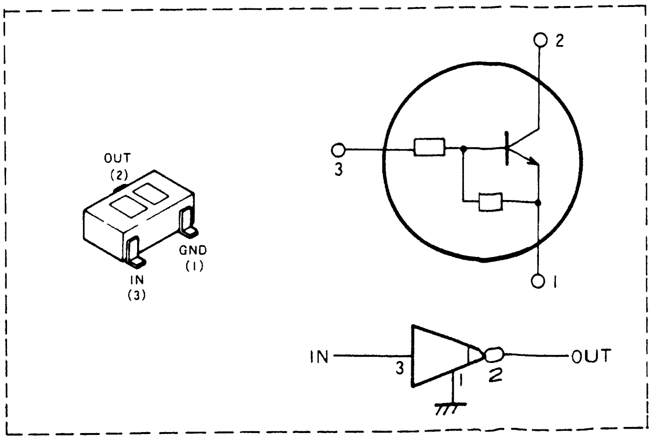
DTC124ES
DTC144WS


GND
(1)
OUT
(2)
IN
(3)
2
3
1
IN
3
1
2
OUT

UN2111
Chip transistor

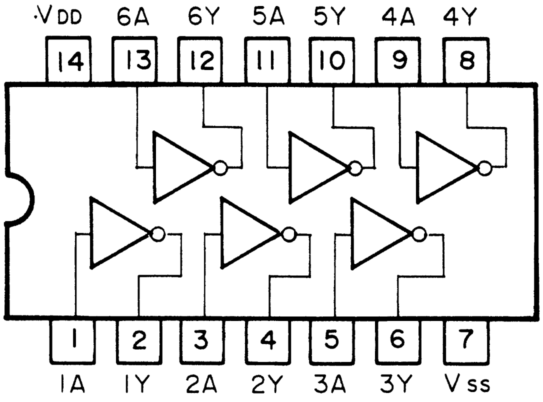

OUT
(2)
+V
(1)
IN
(3)
1
3
2
+V
1
IN
3
2
OUT

UN2211
Chip Transistor

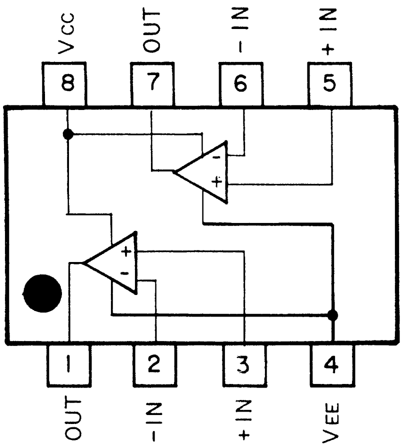

OUT
(2)
GND
(1)
IN
(3)
2
3
1
IN
3
1
2
OUT

Main Unit

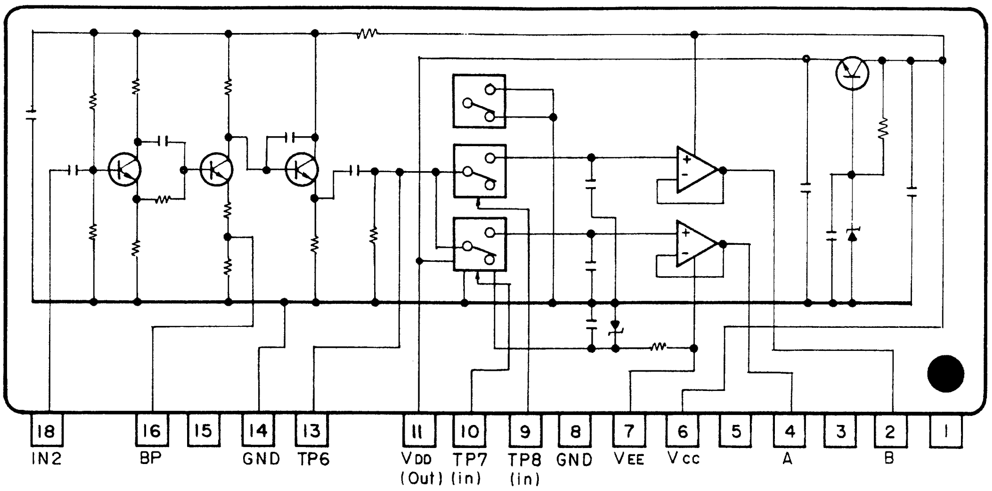
*IC1 : TC40H004F


VDD
6A
6Y
5A
5Y
4A
4Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1Y
2A
2Y
3A
3Y
Vss

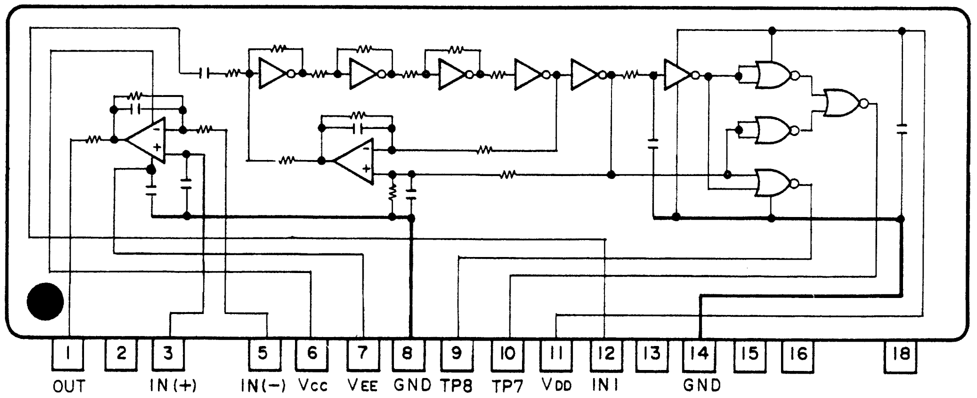
IC2 : NJM4558M


VCC
OUT
− IN
+ IN
8
7
6
5
1
2
3
4
OUT
− IN
+ IN
VEE

IC3 : KHA303


18
IN2
16
BP
15
14
GND
13
TP6
11
VDD
(Out)
10
TP7
(in)
9
TP8
(in)
8
GND
7
VEE
6
Vcc
5
4
A
3
2
B
1

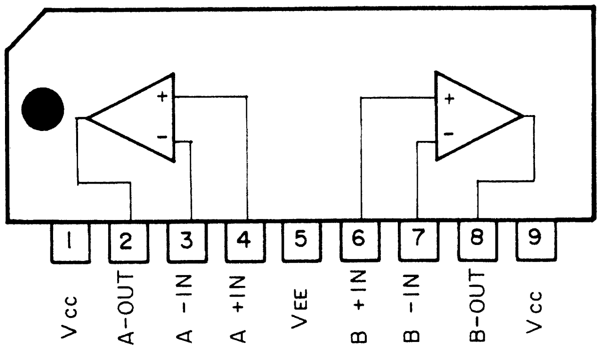
IC4 : KHA304


1
OUT
2
3
IN(+)
5
IN(−)
6
Vcc
7
VEE
8
GND
9
TP8
10
TP7
11
VDD
12
IN1
13
14
GND
15
16
18

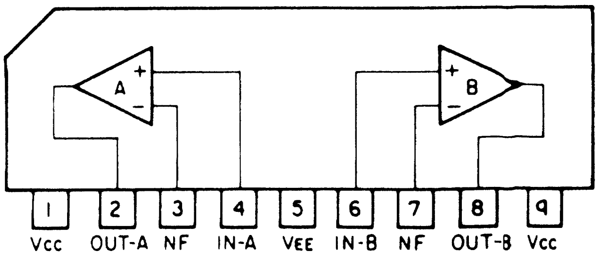
Pin	Pin name	I/O	Function
17	P14 (TEMP)	Input	Temperature rise detection input. At "L" it determines that the temperature is too high, stops operation and displays "HH HHHH."
18	P15 ($\overline{\text{POWER}}$)	Output	DC-DC converter ON/OFF control output. At "L" level, the DC-DC converter turns on and the servo system is supplied with power.
19	P16 ($\overline{\text{MUTING}}$)	Output	Muting control output. At "L" level, the muting circuit turns on, and the audio output drops to GND.
20	P17 (P/$\overline{\text{S}}$)	Output	Spindle motor (START/STOP) control. At "H" level, the spindle motor starts. At "L" level, the spindle motor stops.
21	VDD		Power supply (5 V ±0.25V).
22	P47 (T $\overline{\text{N}}$/W)	Output	While playing the level is "L", and the band is narrow. During search or jump, the level is "H" and the servo band is wide.
23	P46 ($\overline{\text{RA-G}}$)	Output	Normally "H" level, but changes to "L" level during jumps. If pin 16 (R-O/$\overline{\text{C}}$) is "L" level, it adds offset to the carriage servo.
24	P45 ($\overline{\text{DACK}}$)	Input	Data acknowledge input. During communications with the sub-microcomputer PD6029, it receives the data acknowledge from PD6029. Active "L"
25	P44 (DSTB)	Output	Data strobe output. Active "H."
26 ~ 29	P43 (D13) ~ P40 (D10)	Input	Connects to a four-bit bi-directional communications interface and takes data from the data bus.
30	P37 (SOSI)	Input	Sub-code sync pattern input.
31	P 36 (SCQU)	Input	Sub-code Q channel input.
32	P35 (SEL1)	Output	PD8010 function selection
33	P36 (SEL0)	Output	
34 ~ 37	P33 (DO3) ~ P30 (DO0)	Output	Four-bit data output. Data output for PD8010, and data output during communications with PD6029.
38	$\overline{\text{LOAD}}$	Output	Data strobe output for outputting data to PD8010. One-micro-second pulse.
39	PFCK	Input	When the sub-code is read as normal, a 136 μsec. signal (duty: 50%) is input.
40	E	Output	System clock frequency divider output. 1 kHz (duty: 50%), which is one fourth of the system clock frequency, is output to this pin. It is used as the clock for PD8010 clock.

SEL 1	SEL 0	Operation mode
0	0	――――
0	1	Latch "A" select (mainly for FOCUS system control).
1	0	Latch "B" select (mainly for TRACKING system control).
1	1	Counter preset

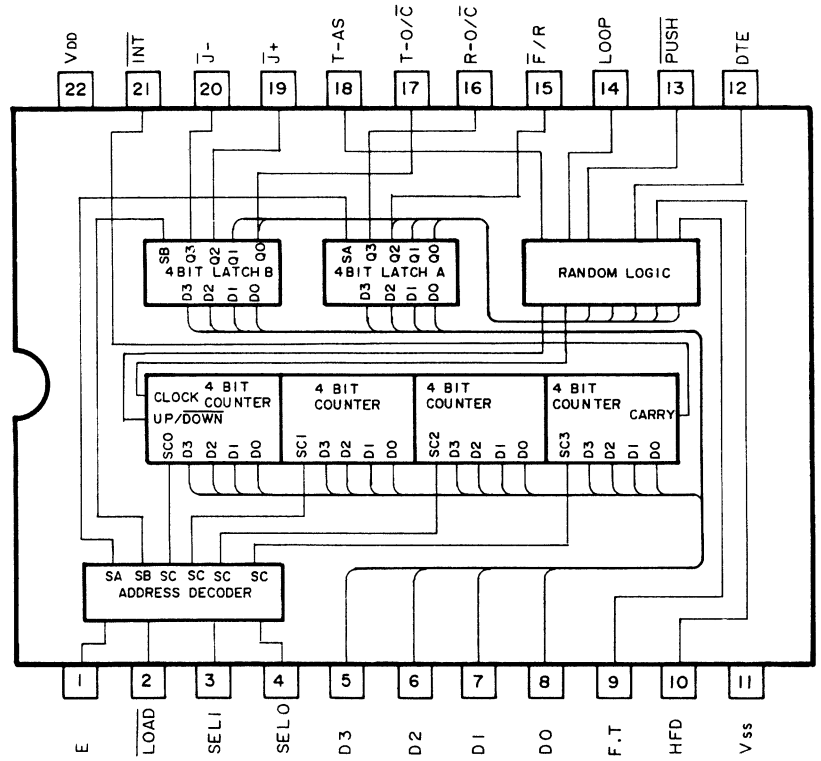
IC4 : NJM2903S



IC5, IC7, IC8 : TA75558S



*IC3 : PD8010

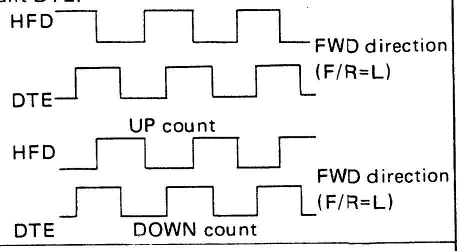
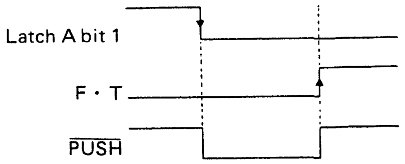
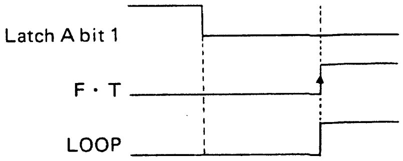

VDD
INT
J-
J+
T-AS
T-O/C
R-O/C
F/R
LOOP
PUSH
DTE
22
21
20
19
18
17
16
15
14
13
12
SB Q3 Q2 Q1 Q0
4 BIT LATCH B
D3 D2 D1 D0
SA Q3 Q2 Q1 Q0
4 BIT LATCH A
D3 D2 D1 D0
RANDOM LOGIC
CLOCK
4 BIT COUNTER
UP/DOWN
SC0 D3 D2 D1 D0
4 BIT COUNTER
SC1 D3 D2 D1 D0
4 BIT COUNTER
SC2 D3 D2 D1 D0
4 BIT COUNTER
CARRY
SC3 D3 D2 D1 D0
SA SB SC SC SC SC
ADDRESS DECODER
1
2
3
4
5
6
7
8
9
10
11
E
LOAD
SEL1
SEL0
D3
D2
D1
D0
F.T
HFD
Vss

The PD8010 is a random access controller which was developed for mobile CD players. Using commands from the microcomputer (PD3036) in can perform:

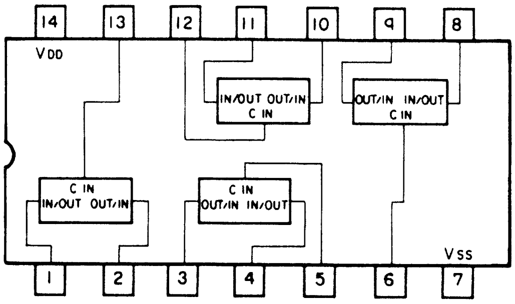
1. Jump operations
2. High-speed random access operations
3. Controls the focus servo circuit.

PD8010 Pin Functions

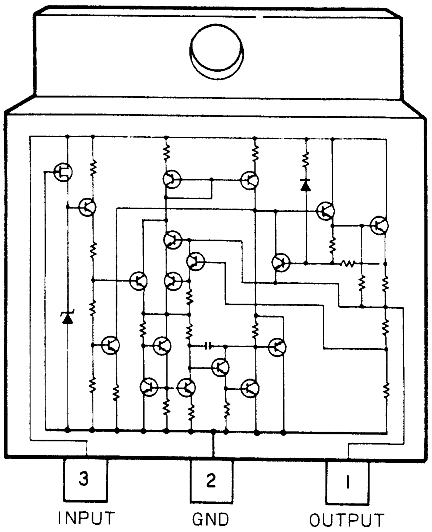
<table>
<tr><th>Pin</th><th>Pin name</th><th>I/O</th><th>Functions</th></tr>
<tr><td>1</td><td>E</td><td>Input</td><td>System clock input (1 MHz)</td></tr>
<tr><td>2</td><td>LOAD</td><td>Input</td><td>Data line strobe input</td></tr>
<tr><td>3</td><td>SEL1</td><td rowspan="2">Input</td><td rowspan="2">Select address input pins for selecting four-bit latch "A," "B," or the 16-bit counter
<table>
<tr><th>SEL 1</th><th>SEL 0</th><th>Operation mode</th></tr>
<tr><td>0</td><td>0</td><td>—</td></tr>
<tr><td>0</td><td>1</td><td>Latch "A" selected</td></tr>
<tr><td>1</td><td>0</td><td>Latch "B" selected</td></tr>
<tr><td>1</td><td>1</td><td>Counter preset</td></tr>
</table></td></tr>
<tr><td>4</td><td>SEL0</td></tr>
<tr><td>5
~
8</td><td>D3
~
D0</td><td>Input</td><td>Four-bit data line (Input pins)</td></tr>
</table>

Pin	Pin name	I/O	Function
9	F · T	Input	FOCUS timing latch clock input pin. Used as input pins for the random logic circuit. (When the random logic circuit operates, it closes the focus servo loop.) It is input into the servo control logic. Signal produced by making binary the envelope of the external RF signal which is 90° out of phase from the TE input. When there is an RF signal, it becomes "H." *The internal 16-bit counter uses the phase differences among the DTE input and the E-OR output of $\overline{\text{F}}$/R and the HFD input, to select UP/$\overline{\text{DOWN}}$ and to count DTE.  HFD FWD direction (F/R=L) DTE UP count HFD FWD direction (F/R=L) DTE DOWN count
10	HFD	Input	
11	VSS		GND
12	DTE	Input	This pin is input into the servo control logic. Input into this pin is the signal produced by making binary the tracking error signal which is 90° out of phase from the HFD pin Signal
13	$\overline{\text{PUSH}}$	Output	Becomes "L" level at the trailing edge of latch A bit 1 output, and returns to "H" level at leading edge of the F · T input pin.  When the level is "L," the lens is pushed out. It draws the lens in at "H" level, and opens the FOCUS speed feedback.
14	LOOP	Output	This is a FOCUS timing latch output pin. When latch A bit 1 is "L" level, the rising edge of the F · T input pin changes it to "H" level.  Used as a signal to open/close the FOCUS LOOP. When the signal is "H" level, the focus loop becomes closed.
15	$\overline{\text{F}}$/R	Output	Sets the carriage direction. "L" level advances toward the outside edge of the disc.
16	R-O/$\overline{\text{C}}$	Output	Acts as a high-speed carriage motion control pin during player search operations. The carriage moves at high speed at "L" level.
17	T-O/$\overline{\text{C}}$	Output	Output pins for opening/closing the carriage servo loop. When "L" level is output from this pin, the external carriage loop closes.
18	T-AS	Output	Acts as a tracking servo loop open/close switch. When the signal is "H" level, the tracking servo loop is closed.
19	$\overline{\text{J+}}$	Output	Outputs "L" level during jumps, and is used as the JUMP+ signal output pin that flows the current for driving the lens toward the center of the disc.
20	$\overline{\text{J–}}$	Output	Outputs "L" level during jumps and is used as the JUMP– signal output pin that flows the current for driving the lens toward the outside edge of the disc.
21	$\overline{\text{INT}}$	Output	Outputs "L" level when it detects a carry when the 16-bit counter is performing a count operation. When new data is preset by the 16-bit counter, it returns to "H" level.
22	VDD		Power supply (+5V).

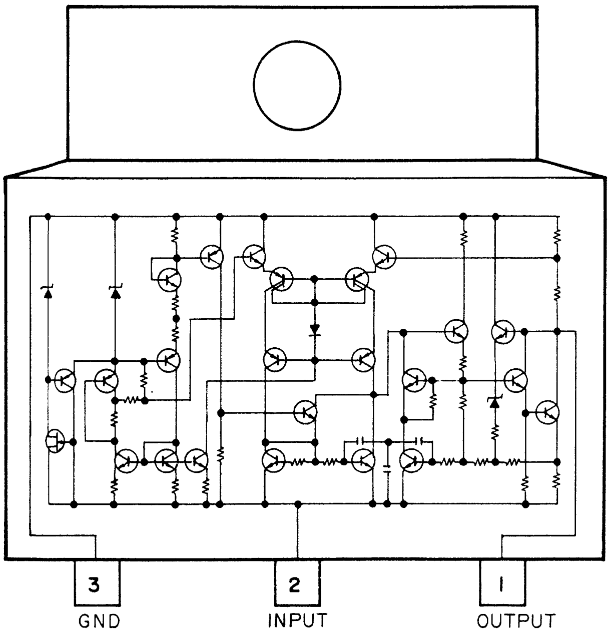
*IC6 : TC4066BP


14
13
12
11
10
9
8
VDD
IN/OUT OUT/IN
C IN
OUT/IN IN/OUT
C IN
C IN
IN/OUT OUT/IN
C IN
OUT/IN IN/OUT
VSS
1
2
3
4
5
6
7

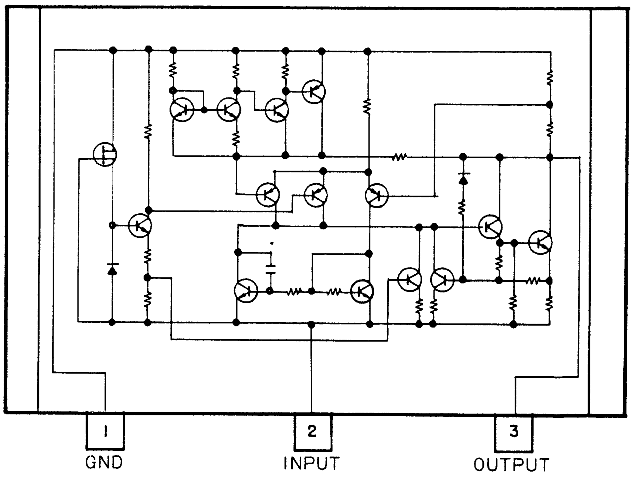
IC9 : NJM78M12A


3
INPUT
2
GND
1
OUTPUT

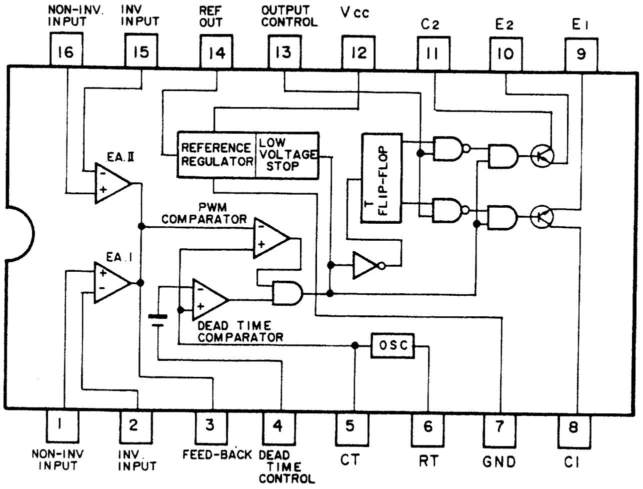
IC10 : NJM79M12A


3
GND
2
INPUT
1
OUTPUT

IC12 : NJM79L05A

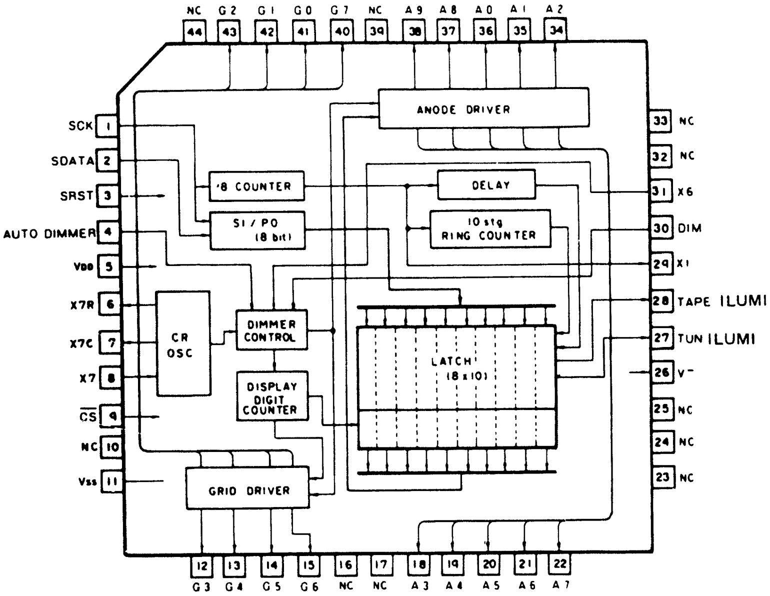

1
GND
2
INPUT
3
OUTPUT

IC50 : μPC494C


NON-INV. INPUT
16
INV INPUT
15
REF OUT
14
OUTPUT CONTROL
13
Vcc
12
C2
11
E2
10
E1
9
EA.II
REFERENCE REGULATOR
LOW VOLTAGE STOP
T
FLIP-FLOP
PWM COMPARATOR
EA.I
DEAD TIME COMPARATOR
OSC
1
NON-INV INPUT
2
INV INPUT
3
FEED-BACK
4
DEAD TIME CONTROL
5
CT
6
RT
7
GND
8
CI

• Display Unit

IC301 : PD7005

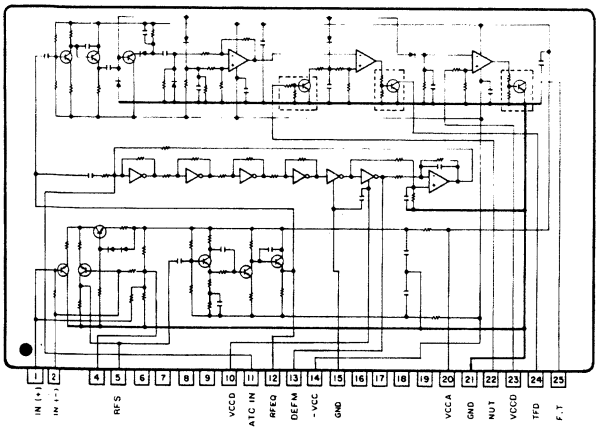

NC 44
G2 43
G1 42
G0 41
G7 40
NC 39
A9 38
A8 37
A0 36
A1 35
A2 34
SCK 1
SDATA 2
SRST 3
AUTO DIMMER 4
VDD 5
X7R 6
X7C 7
X7 8
CS 9
NC 10
Vss 11
33 NC
32 NC
31 X6
30 DIM
29 X1
28 TAPE ILUMI
27 TUN ILUMI
26 V−
25 NC
24 NC
23 NC
12 G3
13 G4
14 G5
15 G6
16 NC
17 NC
18 A3
19 A4
20 A5
21 A6
22 A7
ANODE DRIVER
÷8 COUNTER
DELAY
SI / PO (8 bit)
10 stg RING COUNTER
CR OSC
DIMMER CONTROL
LATCH (8 x 10)
DISPLAY DIGIT COUNTER
GRID DRIVER

PD7005 Pin Functions

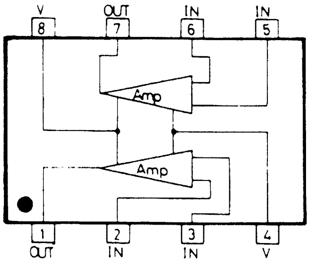
Pin	Pin name	I/O	Function
1	SCK	Input	Serial interface, system lock input.
2	SDATA	Input	Data input.
3	SRST	Input	Reset.
4	AUTO DIMMER		Not in used
5	VDD		+5 V power supply
6 ~ 8	X7R ~ X7		Oscillator circuit
9	CS	Input	Chip selection signal input. Active "L."
10	N.C		
11	VSS		GND
12 ~ 15	G3 ~ G6	Output	FL grid output.
16	N. C		
17	N. C		
18 ~ 21	A3 ~ A6	Output	FL anode output.
22	N. C		
23 ~ 25	N. C		
26	V−	Output	Grid output. Negative voltage output pin for pull-down resistance.
27 ~ 29	TUN illumination TAPE illumination XI		Not in used
30	DIM	Input	The LEDs become dark when ILLUMI+B is applied.
31 ~ 33	N. C		
34 ~ 37	A2 A1 A0 A8	Output	FL anode output.
38 ~ 40	N. C		
41 ~ 43	G0 ~ G2	Output	FL grid output.
44	N. C		

● Signal Processor Unit

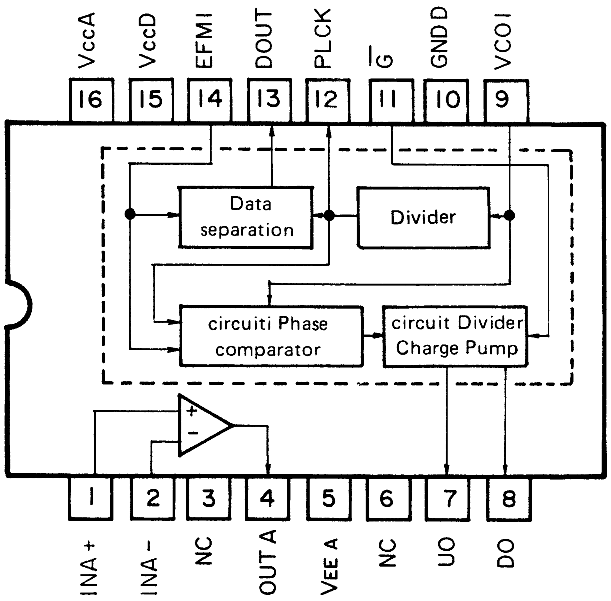
IC1 : KHA301


1
2
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
IN (+)
IN (−)
RFS
VCCD
ATC IN
RFEQ
DEFM
-VCC
GND
VCCA
GND
NUT
VCCD
TFD
F.T

IC2, IC7 : NJM4558DD


V
OUT
IN
IN
8
7
6
5
Amp
Amp
1
2
3
4
OUT
IN
IN
V

IC3 : TD6315AP

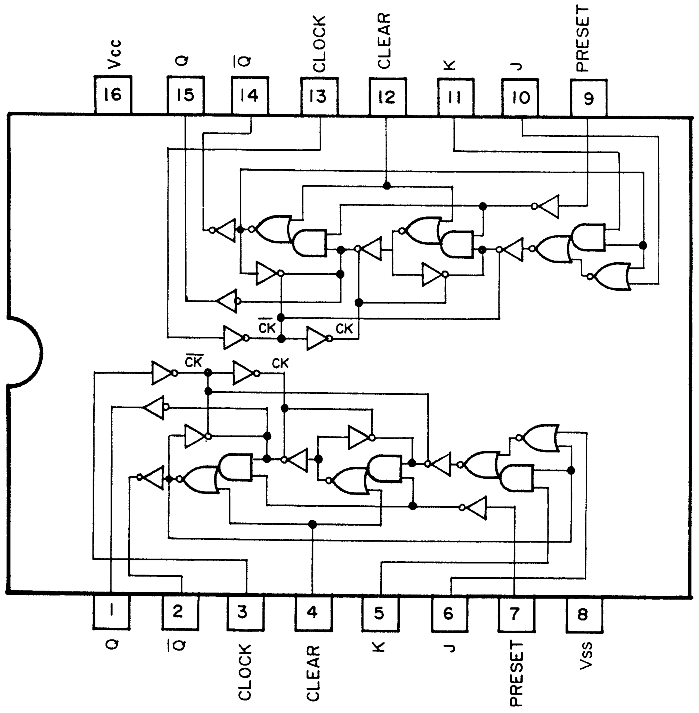

VccA
VccD
EFMI
DOUT
PLCK
G
GND D
VCOI
16
15
14
13
12
11
10
9
Data separation
Divider
circuiti Phase comparator
circuit Divider Charge Pump
+
−
1
2
3
4
5
6
7
8
INA +
INA −
NC
OUT A
VEE A
NC
UO
DO

TD6315AP Pin Functions

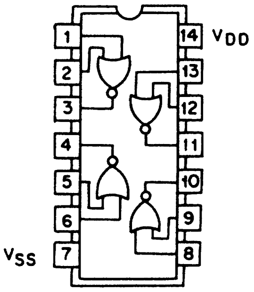
Pin	Pin name	I/O	Function
1	INA+	Input	Internal operational amplifier + input.
2	INA−	Input	Internal operational amplifier − input.
3	N. C		Unconnected. Has the same electric potential as INA+.
4	OUTA	Output	Internal operation amplifier output.
5	VEEA		GND
6	N. C		Unconnected. Has the same electric potential as INA+.
7	UO	Output	Charge pump up signal output.
8	DO	Output	Charge pump down signal output.
9	VCOI		VCO input.
10	GNDD		Digital GND
11	$\overline{G}$	Input	Input pins which make charge pump output UO and DO high impedance. When this pin is "L" level, it enters high impedance mode, and holds the VCO frequency.
12	PLCK	Output	Clock for separating data generated from DEFM input signals by the PLL circuit.
13	D OUT	Output	EFMI signal output.
14	EFMI	Input	Input pin for the digital signal (EFMI) that is produced when the RF signal reproduced from the disc goes through the data slicer.
15	Vcc D		Digital power supply (+5 V).
16	Vcc A		Analog power supply (+12 V).

Pin	Pin name	I/O	Function
29	ALGC	Input	Fixed to "L" in this product.
30 ≀ 33	ATT0 ≀ ATT3	I/O I/O	Internal digital attenuator level monitor and external control pin.
34	$\overline{\text{MUT1}}$	Input	Muting control. At "L" level, the attenuation quantity increases, and at "H" level the attenuator quantity decreases.
35	$\overline{\text{MUTO1}}$	Output	When a burst error of 64 frames or more, or the jitter absorption memory buffer over is detected, "L" level is output.
36	$\overline{\text{MUTO2}}$	Output	"L" level is output when three frames of de-interleave error is detected.
37	P/S SE	Input	Output data parallel/serial selection. Parallel output at "L" level, and serial output at "H" level.
38 ≀ 46	DA0 ≀ DA6	Output Output	(Not in use.)
47	SDATA	Output	When pin 37 is "L" level, it outputs an eight-bit data starting from the MSB. When pin 37 is "H" level, it outputs serial data starting from the MSB.
48	BCK	Output	Bit clock output pin. Serial data is output in synchronization with the clocks trailing edge. (1.4112 MHz)
49	MLCK	Output	MSB/LSB clock output pin. The clock output is 1/8 the frequency of BCK and is used to set the clock when outputting eight-bits parallel data. (176.4 KHz)
50	$\overline{\text{WDCK}}$	Output	Word clock output pin. The clock output is 1/16 the frequency of BCK and indicates the output period of one word. (88.2 kHz)
51	L/RG	Output	Sampling frequency output pin. The clock output is 1/2 the frequency of $\overline{\text{WDCK}}$ and indicates the data output Lch/Rch. (44.1kHz) "L" level is Lch, and "H" level is Rch.
52	X-0	Output	Crystal oscillator connector pin. (8.4672 MHz)
53	X-1	Input	
54	CKSE	Input	Clock select pin. It selects the frequency of the crystal oscillator: At "H" level or when open it's 8.4672 MHz, and at "L" level, it's 4.2336 MHz.
55	CK4M	Output	4 MHz clock output pin. (Not in use.)
56	CK2M	Output	2 MHz clock output pin. (2.1168 MHz) Used as TC9178F clock output.
57	TESI	Input	Test pin. Normally "H" level or open.
58	TES2		
59	COFS	Output	Frame period output pin. Correction frame period output.
60	DSLP	Output	Data status latch output pin.
63	DAST	Output	Data status output pin. Outputs the contents of the results of the jitter absorption memory and the C1, C2 error detection in the form of bit serial output.
64	DIV−	Output	Buffer amplifier output pin. It outputs "H" level when the jitter absorption memory buffer capacity ±4 frames reaches +2 or +3 frames. This output connects to TC9178F (DIV−) and reduces the disc motor revolutions (rpm).
65	DIV+	Output	Buffer down output pin. It outputs "H" level when the jitter absorption memory buffer capacity ±4 frames reaches −2 or −3 frames. This output connects to TC9178F (DIV+) and increases the disc motor revolutions (rpm).
66	BUSE	Input	Buffer select input pin. It selects the output conditions for DIV-/DIV+. Its output range at "H" level is ± 2 and at "L" level ±3 frames.

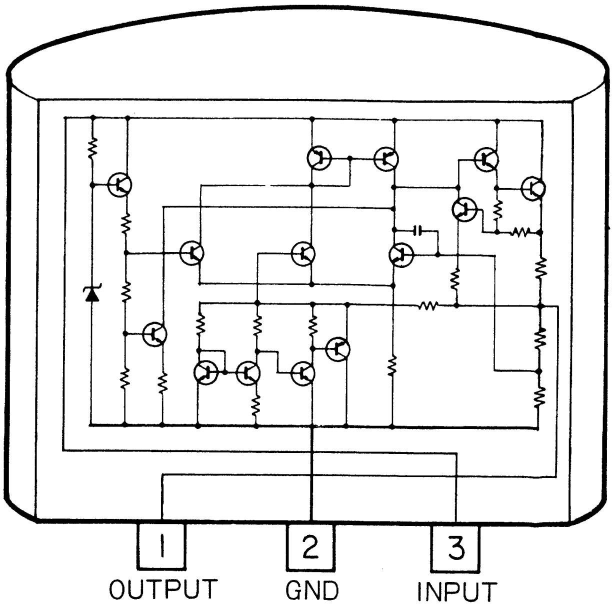
*IC8 : TC4027BP


Vcc
Q
Q̄
CLOCK
CLEAR
K
J
PRESET
16
15
14
13
12
11
10
9
CK̄
CK
CK̄
CK
1
2
3
4
5
6
7
8
Q
Q̄
CLOCK
CLEAR
K
J
PRESET
Vss

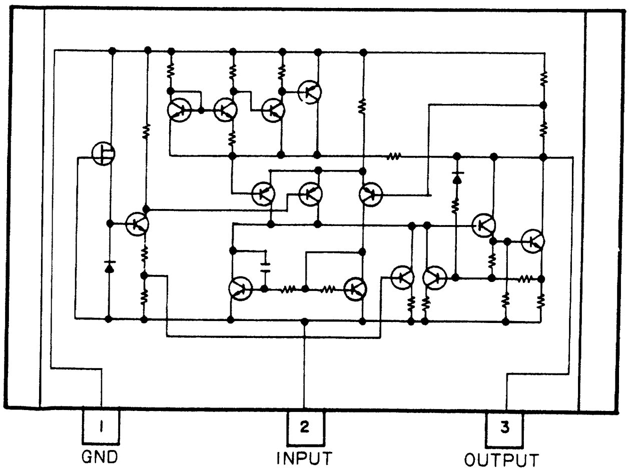
IC9 : TC4001BP


1
2
3
4
5
6
7
14
13
12
11
10
9
8
VDD
VSS

IC10 : NJM78L08A

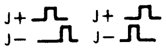

1
OUTPUT
2
GND
3
INPUT

IC11 : NJM79L09A

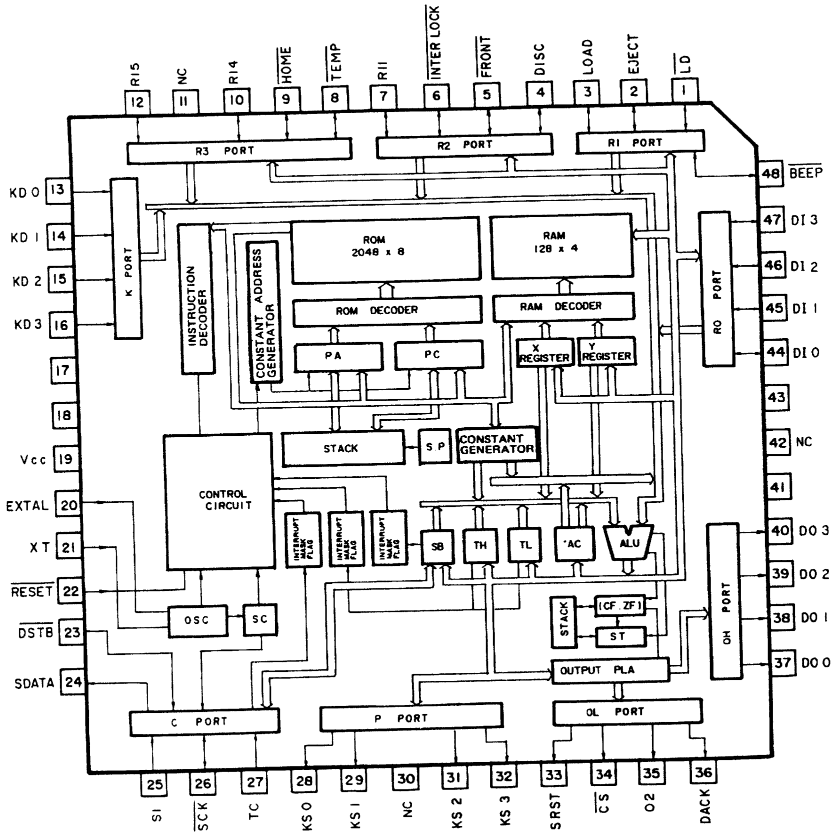

1
GND
2
INPUT
3
OUTPUT

• Circuit Diagram Abbreviations

Abbrevia-tion	Detail	Purpose	Connector line stage	Comments
ACC	ACCESSORY	Main power supply	14.4V	
AUX B	AUX +B	Informs that DC operation is in progress. +B OUTPUT	14.2V	Output from AUX connector pin 5.
CLR	CLEAR	Reset input for external IC2 (PD3036)	7V 0V 30ms "L"	Output from the clear key (S9).
COFS	CORRECTION FRAME SYNC	Correction frame synchronise output	Photo 1	External monitor, IC6 (TC9179F) pin 59.
CM	CARRIAGE MOTOR	Pickup unit carriage motor	Changes at about CM⊕7V and CM⊖ 6V	
CS	CHIP SELECT	Activates the display driver (PD7005)	Photo 2	IC6 (PD6029) pin 34 → IC301 (PD7005) pin 9.
D	DATA (D0 ~ D3)	Data from the system controller (PD3036)	Photo 3	IC2 (PD3036) → IC3 (PD8010) → IC6 (PD6029)
DACK	DATA ACKNOWLEDGE	Acknowledges receipt of data output by IC6 (PD6029)	Photo 4	PD6029 pin 36 → PD3036 pin 24
DAST	DATA STATUS	Outputs data status output, jitter absorption memory and the error detection results of C1 and C2 in bit serial.	Photo 5	External monitor IC6(TC9179F) pin 63
DCNT	DC-DC CONVERTER CONTROL	Display power supply drive output. (Turns on the ACC assemblyDC-DC converter.)	5V— ON 0V OFF	IC6 (PD6029) pin 6 "L" level, DCNT is "H" level.
DIS B	DISABLE +B	A +B for externally stopping the CD operation.	14.2V	Input from AUX connector pin 6.
DSLP	DATA STATUS LATCH PALUS	Data status latch signal output.	Photo 6	External monitor IC6(TC9179F) pin 60.
DSTB	DATA STROBE	The system controller (IC2: PD3036) using this signal, informs IC6 that the data on data bus DO to D3 is valid, prompting IC6 to receive the data.	Photo 4	PD3036 pin 25 → PD6029 pin 23.
FDRI	FOCUS DRIVER INPUT	Input to the focus actuator and the driver.	Photo 7	Servo unit Q38 and Q39 input.
FDRO	FOCUS DRIVER OUTPUT	Focus actuator and driver output.	Photo 8	Servo unit Q38 and Q39 output.
FE	FOCUS ERROR	Focus error detection signal.	Photo 9	
FEVR	FOCUS ERROR VR OUTPUT	Monitor output controlled with the focus error signal volume.		
FG	FREQUENCY GENERATOR	Pulse output in proportion to the spindle motor rpms. (For detecting uncontrolled rotation of the motor.)	Photo 10	
FOS	FOCUS OFFSET	Focus offset standard voltage.	Approximately −1.8 V	
FRONT	FRONT	Detects whether or not the disc unit plate is in front. (Detects eject completion.)	5V "L" 0V EJECT	Operated with front SW (S10).
FRTN	FOCUS RETURN	Focus actuator return voltage.	See adjustment methods.	
FSG	FOCUS SG INPUT	Input pin for the oscillator when adjusting the servo gain.	——	
FT	FOCUS TRIGGER	Detects focal point and monitors the focus system operations.	5V Normally "H" 0V	OUTPUT from IC1 (KHA301) pin 25 → IC2(PD3036) pin 16 IC3(PD8010)pin 9
FY	FOCUS Y OUTPUT	Connecting pin for phase meter during focus servo gain adjustment.	——	
HFD	HIGHT FREQUENCY DETECTOR	Detected RF signal	5V There is an "H" RF signal 0V	Output from IC1 (KHA301) pin 24 → IC3 (PD8010) pin 10

Abbreviation	Detail	Purpose	Condition on the connector line	Comments
HOME	HOME	Detects whether or not the pickup is at home position.	5V 0V "L" home position.	By means of HOME SW (S13) → IC6 (PD6029) pin 4.
ILL	ILLUMINATION	Night illumination power supply	14.4V	
J	JUMP (J+, J–)	Drives the lens toward the center of the disc during pickup jumps.	 (Toward record center) (Toward record outside edge)	Output from IC3 (PD8010) pin 19 and 20.
KD	KEY DATA (KD1 ~ KD3, KS0 ~ KS3)	Data for each key input.	KD1 to KD3 are normally "H" level. KSO to KS3 are normally "L" level. Data is entered at the time of key input. Photo 11.	
LDM	LOADING MORTOR	Drive motor for loading the disc into the set and then unloading it.	LDM– 0V LDM+ 6.5V loading PLAY	
LOOP	FOCUS LOOP CONTROL	Output to open and close the focus loop.	"H": open; "L": closed. Usually "L" level.	Output from IC (PD8010) pin 14.
MUT	MUTING	Inhibits output from all circuits	"L": MUT ON	
PFCK	PLAY BACK FRAME SYNC CLOCK	Signal output for whether or not the sub-code is being read normally.	Photo 12 Duty ratio 50%	IC4 (TC9178F) pin 31 → IC3 (PD3036) pin 39.
P/$\overline{S}$	PLAY/STOP	Drives and stops the spindle motor.	"H": drive; "L": stop.	IC (PD3036) pin 20 → IC4 (TC9178F) pin 21.
PUSH	PUSH	Signal for pushing out and bringing in the object lens during focus signal control.	At "L" the lens is drawn in. It's normally "L" level.	Output from IC3 (PD8010) pin 13.
RFOUT	RF OUT	RF signal output	Photo 13	From the player section to the signal processor.
SCQU	SUB CODE Q & U	Sub-code Q channel input pin.	Photo 15	IC4 (TC9178F) pin 24 → IC2 (PD3036) pin 31.
SOS 1	SUB CODE SYNCH S0 AND S1	Sub-code synchronize pattern input pin.	Photo 14	IC4 (TC9178F) pin 27 → IC2 (PD3036) pin 30.
SWD5	SWITCHED 5 VOLTS	Power supplied to other ICs with commands from the system controller.	5V	The SWD5 line goes on when IC2 (PD3036) pin 11 is "H" level.
T-AS	TRACKING ANALOGUE SWITCH	For opening and closing the tracking servo loop.	Closed at "L." Normally "L."	Output from IC3 (PD8010) pin 18.
TDRI	TRACKING DRIVER INPUT	Tracking actuator driver input.	Photo 16	Servo unit Q36, Q37
TDRO	TRACKING DRIVER OUTPUT	Tracking actuator driver output.	Photo 17	Servo unit Q36, Q37
TE	TRACKING ERROR	Tracking error detection signal.	Photo 18	
TRTN	TRACKING RETURN	Tracking actuator return voltage.	See adjustment methods.	
TSG	TRACKING SG INPUT	Input pin for oscillator during tracking servo gain adjustment.	————	
T-$\overline{W}$/N	TRACKING WIDE/NARROW	Tracking servo band switch.	5V N Normally "H." 0V W	
TY	TRACKING Y OUTPUT	Connecting pin for phase meter during tracking servo gain adjustment.	————	
VC	VOLTAGE CONTROL	Spindle motor control voltage.	RPMs are decided by one voltage less than or equal to 5 V.	
VM	VOLTAGE FOR MORTOR	loading motor driver IC7 (M54546L) power supply.	6.8V	
WDCK	WORD CLOCK	Word clock output.	Photo 19	Output from IC6 (TC9179F) pin 50 external monitor.

*IC6 : PD6029

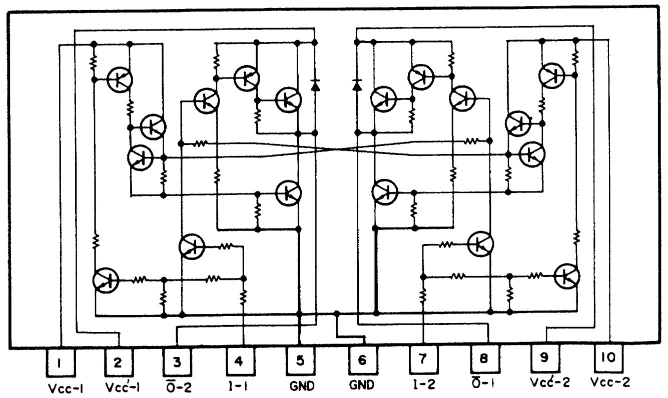

R15
NC
R14
$\overline{\text{HOME}}$
$\overline{\text{TEMP}}$
R11
$\overline{\text{INTER LOCK}}$
$\overline{\text{FRONT}}$
DISC
LOAD
EJECT
$\overline{\text{LD}}$
12
11
10
9
8
7
6
5
4
3
2
1
R3 PORT
R2 PORT
R1 PORT
48 $\overline{\text{BEEP}}$
KD 0 13
KD 1 14
KD 2 15
KD 3 16
17
18
Vcc 19
EXTAL 20
XT 21
$\overline{\text{RESET}}$ 22
$\overline{\text{DSTB}}$ 23
SDATA 24
K PORT
INSTRUCTION DECODER
CONSTANT ADDRESS GENERATOR
ROM 2048 x 8
RAM 128 x 4
ROM DECODER
RAM DECODER
PA
PC
X REGISTER
Y REGISTER
RO PORT
47 DI 3
46 DI 2
45 DI 1
44 DI 0
43
42 NC
41
40 DO 3
39 DO 2
38 DO 1
37 DO 0
STACK
S.P
CONSTANT GENERATOR
CONTROL CIRCUIT
INTERRUPT MASK FLAG
INTERRUPT MASK FLAG
INTERRUPT MASK FLAG
SB
TH
TL
AC
ALU
STACK
(CF. ZF)
ST
OSC
SC
OH PORT
OUTPUT PLA
C PORT
P PORT
OL PORT
25
26
27
28
29
30
31
32
33
34
35
36
SI
$\overline{\text{SCK}}$
TC
KS0
KS1
NC
KS2
KS3
SRST
$\overline{\text{CS}}$
O2
DACK

PD6029 Pin Functions

Pin	Pin name	I/O	Function
1	$\overline{\text{LD}}$	Output	Turns the laser diode on and off. It turns on at "L" level.
2	EJECT	Output	Reverses the loading motor, and ejects the disc.
3	LOAD	Output	Runs the loading motor forward and loads the disc.
4	DISC	Input	Detects whether or not there is a disc loaded. Inputs "H" level when a disc has been loaded.
5	$\overline{\text{FRONT}}$	Input	Detects whether or not the disc plate unit (part of the mechanism unit) is in front. It indicates the completion of ejection.
6	$\overline{\text{INTFR LOCK}}$	Input	Detects whether or not the disc plate unit is in back and indicates the completion of loading.
7	N.C		
8	$\overline{\text{TEMP}}$	Input	Detects rises in internal temperature.
9	$\overline{\text{HOME}}$	Input	Detects whether or not the pickup is in the home position.
10 12	N.C		
13 16	KD0 ∫ KD3	Input	Takes in four-bit data in response to the key that has been pressed.
17	N.C		
18	N.C		
19	Vcc		+5V power supply
20	EXTAL		Built-in clock generator for outside circuits.
21	XT		
22	$\overline{\text{RESET}}$	Input	Is reset at "L" level.

Pin	Pin name	I/O	Function
23	$\overline{\text{DSTB}}$	Input	This is an external interrupt input and is used as a data strobe during communications.
24	SDATA	Output	This is a serial transfer line for display data to IC301 (PD7005).
25	SI	Input	Switches from normal mode to the chip check mode during program reset ("H" level is normal mode, "L" level is chip check mode.)
26	SCK	Output	Synchronous timing output during serial transfer.
27	N.C		
28	KS0	Output	Key SCAN output for input key sense.
29	KS1		
30	N.C		
31	KS2	Output	Key SCAN output for input key sense.
32	KS3		
33	SRST	Output	Reset output for IC301 (PD7005)
34	$\overline{\text{CS}}$	Output	Output for making IC301 active.
35	N.C.		
36	DACK	Output	Output used to acknowledge data in communications.
37 40	DO0 ∫ DO3	Output	Four-bit parallel data line used during communications.
41	Vss		GND
42	N.C		
43	N.C		
44 47	DI0 ∫ DI3	Input	Four-bit parallel input data line.
48	$\overline{\text{BEEP}}$	Output	Controls the beep generator and beeps at "L" level. (30 mSec.)

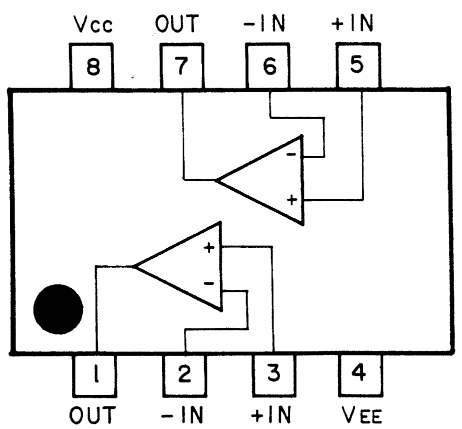
IC7 : M54546L


1
2
3
4
5
6
7
8
9
10
Vcc-1
Vcc'-1
$\overline{\text{O}}$-2
I-1
GND
GND
I-2
$\overline{\text{O}}$-1
Vcc'-2
Vcc-2

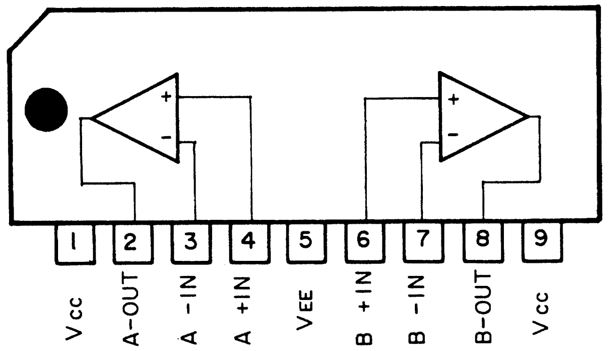
M54546L Pin Functions

Pin	Pin name	I/O	Function
1	Vcc-1		Power supply
10	Vcc-2		
2	Vcc'-1		Output power supply, motor output power supply.
9	Vcc'-2		
3	O-2	Output	Becomes "H" level during EJECT.
8	O-1	Output	Becomes "H" level during LOAD.
4	I-1	Input	Becomes "H" level during LOAD.
7	I-2	Input	Becomes "H" level during EJECT.
5	GND		GND
6	GND		

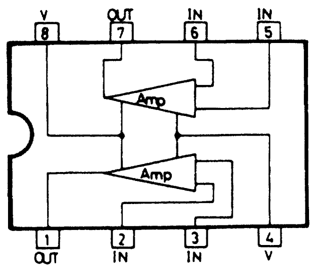
IC5 : NJM2904D


Vcc
OUT
-IN
+IN
8
7
6
5
1
2
3
4
OUT
-IN
+IN
VEE

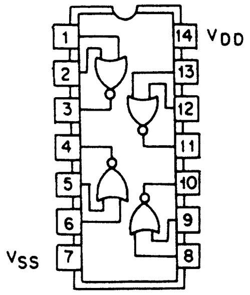
IC9 : NJM2903M


1
2
3
4
5
6
7
8
9
Vcc
A-OUT
A -IN
A +IN
VEE
B +IN
B -IN
B-OUT
Vcc

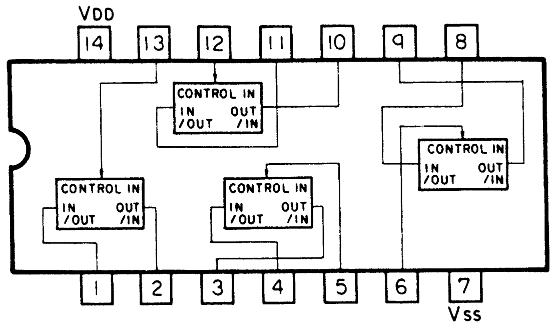
IC102~IC104 : TA75558P


V
OUT
IN
IN
8
7
6
5
Amp
Amp
1
2
3
4
OUT
IN
IN
V

*IC8 : TC4001BF

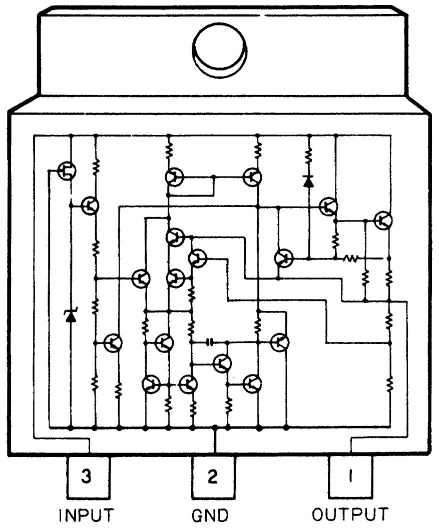

1
2
3
4
5
6
7
14
13
12
11
10
9
8
VDD
VSS

*IC101 : TC4066BP

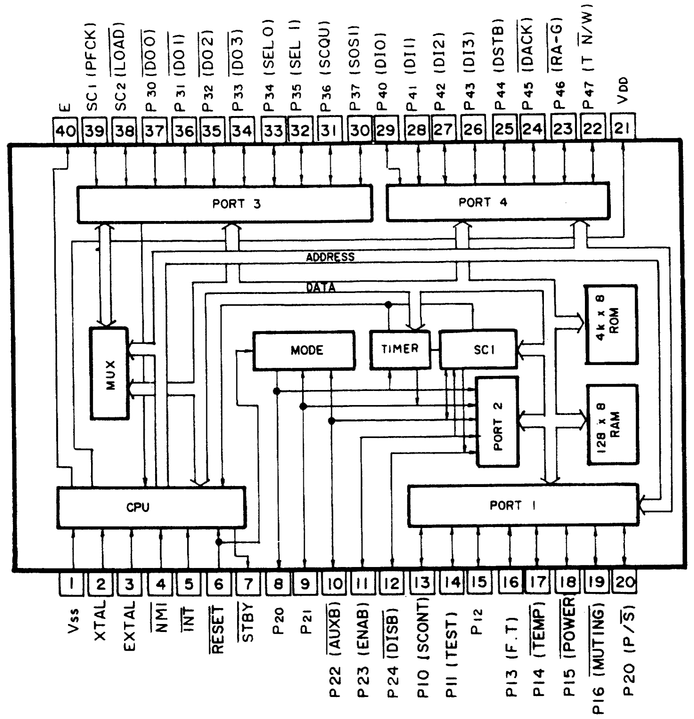

VDD
14
13
12
11
10
9
8
CONTROL IN
IN OUT
/OUT /IN
1
2
3
4
5
6
7
Vss

- **Servo Unit**

IC1, IC11 : NJM78M05A


3
2
1
INPUT
GND
OUTPUT

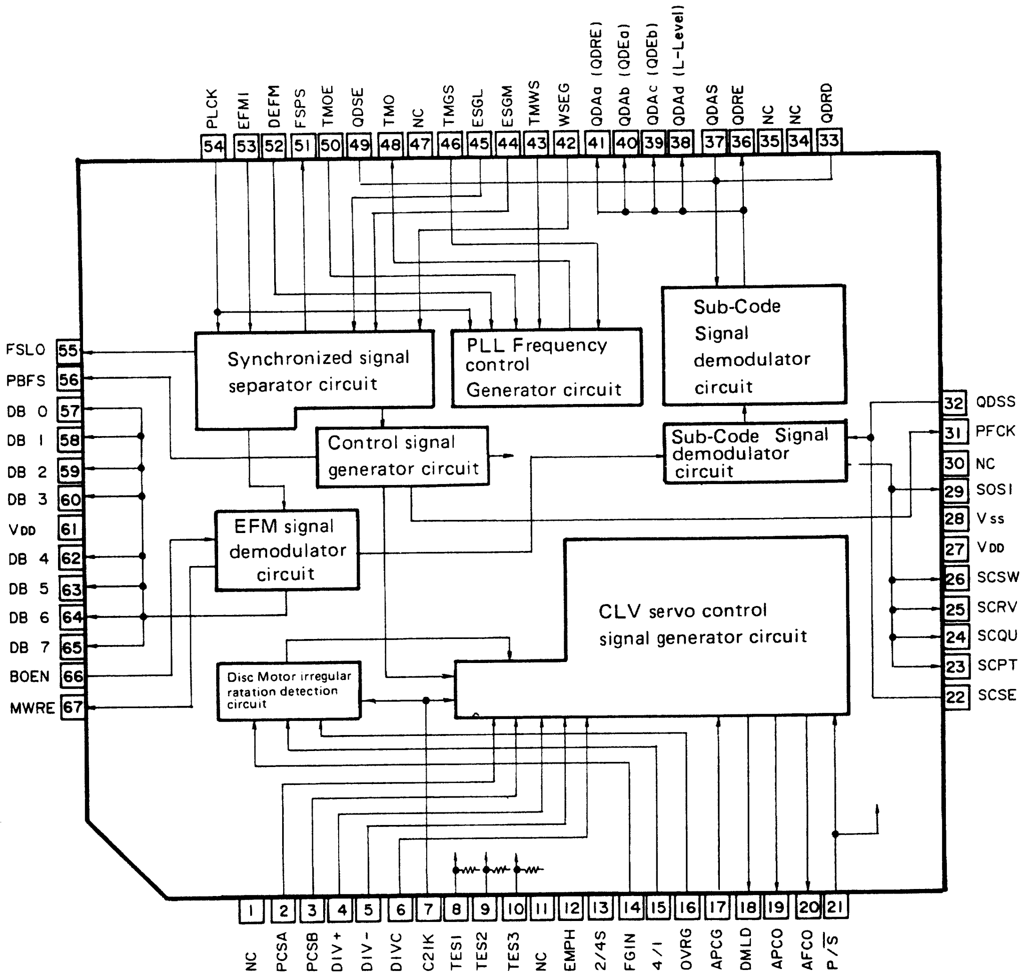
*IC2 : PD3036


E
SC1 (PFCK)
SC2 (LOAD)
P30 (DO0)
P31 (DO1)
P32 (DO2)
P33 (DO3)
P34 (SEL 0)
P35 (SEL 1)
P36 (SCQU)
P37 (SOSI)
P40 (DI0)
P41 (DI1)
P42 (DI2)
P43 (DI3)
P44 (DSTB)
P45 (DACK)
P46 (RA-G)
P47 (T N/W)
VDD
40
39
38
37
36
35
34
33
32
31
30
29
28
27
26
25
24
23
22
21
PORT 3
PORT 4
ADDRESS
DATA
MUX
MODE
TIMER
SCI
4k x 8 ROM
128 x 8 RAM
PORT 2
CPU
PORT 1
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
Vss
XTAL
EXTAL
NMI
INT
RESET
STBY
P20
P21
P22 (AUXB)
P23 (ENAB)
P24 (DISB)
P10 (SCONT)
P11 (TEST)
P12
P13 (F.T)
P14 (TEMP)
P15 (POWER)
P16 (MUTING)
P20 (P/S)

PD3036 Pin Functions

Pin	Pin name	I/O	Function
1	Vss		GND
2	XTAL	Input	System clock crystal (4 MHz) connector.
3	EXTAL	Output	
4	$\overline{NMI}$	Input	A non-maskable Interrupt input pin. This pin orders the unit into the back up mode when a power supply cut-off is detected.
5	$\overline{INT}$	Input	Interrupt input. A signal for stopping track counting is input to this pin. (Active "L".)
6	$\overline{RESET}$	Input	Reset input. Connects to the reset circuit.
7	$\overline{STBY}$	Input	Standby control input. When this pin is turned to "L" level, the current consumption of the CPU during back-up can be reduced. It is connected directly to pin 13 and goes through pin 4 ($\overline{NMI}$), and R9, and operates as follows: 1. When pin 4 becomes "L" level, the power supply is cut off. 2. When PD3036 detects a power supply cut-off, it starts to save RAM data, and prepares to go into backup mode. 3. When preparations are complete, it changes pin 13 (SCONT) to high impedance. 4. When pin 13 becomes high impedance, pin 7 ($\overline{STBY}$) is brought down to "L" level by R9 and becomes a low-power consumption back up. Back-up mode can be changed back to normal operation with input from pin 6 ($\overline{RESET}$).
8	P20		Connects to +5V line.
9	P21		
10	P22 ($\overline{AUXB}$)	Output	Commands AUX+B output. Outputs "L" level when player is in operation.
11	P23 (ENAB)	Output	Commands SWD+5 V output. This becomes "H" level and maintains "H" level 150 ms after RESET is input during CPU operation. It also issues a start command to PD6029.
12	P24 ($\overline{DISB}$)	Input	DISB detection input. Connects to the AUX control circuit and detects DISB at "L" level.
13	P10 (SCONT)	Output	Standby control output. Normally "H" level.
14	P11 (TEST)	Input	Test mode command input The chip goes into test mode when it is reset while this pin is "L".
15	P12		Connects to +5 V line.
16	P13 (F · T)	Input	Focus trigger input. Acts as a performance monitor for the FOCUS system, it determines the FOCUS system to be normal at "H" level.

* IC4 : TC9178F

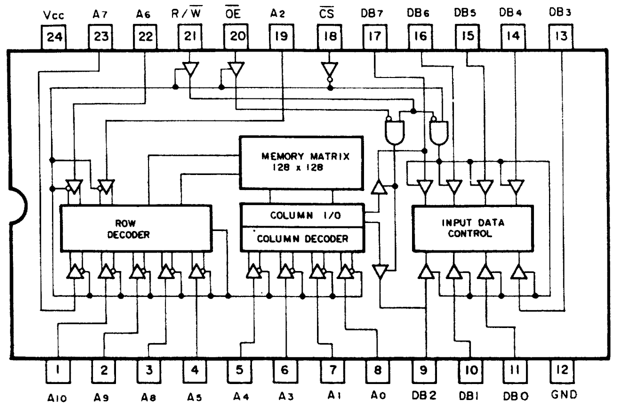

PLCK 54
EFMI 53
DEFM 52
FSPS 51
TMOE 50
QDSE 49
TMO 48
NC 47
TMGS 46
ESGL 45
ESGM 44
TMWS 43
WSEG 42
QDAa (QDRE) 41
QDAb (QDEa) 40
QDAc (QDEb) 39
QDAd (L-Level) 38
QDAS 37
QDRE 36
NC 35
NC 34
QDRD 33
FSLO 55
PBFS 56
DB 0 57
DB 1 58
DB 2 59
DB 3 60
VDD 61
DB 4 62
DB 5 63
DB 6 64
DB 7 65
BOEN 66
MWRE 67
32 QDSS
31 PFCK
30 NC
29 SOSI
28 Vss
27 VDD
26 SCSW
25 SCRV
24 SCQU
23 SCPT
22 SCSE
1 NC
2 PCSA
3 PCSB
4 DIV+
5 DIV-
6 DIVC
7 C21K
8 TESI
9 TES2
10 TES3
11 NC
12 EMPH
13 2/4S
14 FGIN
15 4/1
16 OVRG
17 APCG
18 DMLD
19 APCO
20 AFCO
21 P/S̄
Synchronized signal separator circuit
PLL Frequency control Generator circuit
Sub-Code Signal demodulator circuit
Control signal generator circuit
Sub-Code Signal demodulator circuit
EFM signal demodulator circuit
CLV servo control signal generator circuit
Disc Motor irregular ratation detection circuit

TC9178F Pin Functions

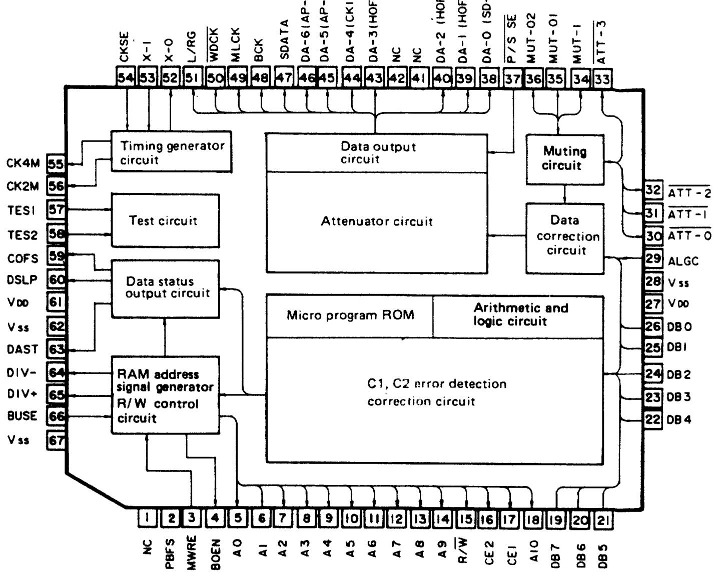
<table>
<tr><th>Pin</th><th>Pin name</th><th>I/O</th><th>Function</th></tr>
<tr><td>1</td><td>N. C</td><td></td><td></td></tr>
<tr><td>2</td><td>PCSA</td><td>Input</td><td>CLV servo control APS signal circuit phase comparison frequency selector.</td></tr>
<tr><td>3</td><td>PCSB</td><td>Input</td><td>Phase comparison frequency fc = 7.35 kHz (frame synchronizing signal/N).
<table><tr><th>PCSA</th><th>PCSB</th><th>N</th><th>fc (Hz)</th></tr><tr><td>L</td><td>L</td><td>6</td><td>1225</td></tr></table></td></tr>
<tr><td>4</td><td>DIV+</td><td>Input</td><td rowspan="3">Inputs to these pins changes the reference frequency for comparing phases in the CLV servo control signal APC generator circuit. It is input in the form of a buffer memory status signal from TC9179F. The amount of variation can be selected using the DIVC pin.
<table><tr><th>DIV+</th><th>DIV−</th><th>DIVC</th><th>Standard frequency division ratio</th><th>Disc motor revolutions</th></tr><tr><td>H</td><td>L</td><td>L</td><td>1/287.5</td><td>Speed up</td></tr><tr><td>L</td><td>H</td><td>L</td><td>1/288.5</td><td>Slow down</td></tr><tr><td>L</td><td>H</td><td></td><td>1/288</td><td></td></tr></table></td></tr>
<tr><td>5</td><td>DIV−</td><td>Input</td></tr>
<tr><td>6</td><td>DIVC</td><td>Input</td></tr>
<tr><td>7</td><td>C21K</td><td>Input</td><td>2.1188 MHz input. Duty 50%.
The crystal oscillator frequency (8.4672 MHz) from TC9179F is frequency divided by four and input into this pin.</td></tr>
<tr><td>8
∫
10</td><td>TES 1
∫
TES 3</td><td>Input</td><td>Test input.
Normal operation at "H" level or when open. (Not in use.)</td></tr>
<tr><td>11</td><td>N. C</td><td></td><td></td></tr>
<tr><td>12</td><td>EMPH</td><td>Output</td><td>This output pin determines whether or not there is any emphasis displayed by the sub-code signal Q control bit.
The de-emphasis is on at "H" level.</td></tr>
<tr><td>13</td><td>N. C</td><td></td><td></td></tr>
<tr><td>14</td><td>FGIN</td><td>Input</td><td>Input pin for the disc motor FG pulse.
Either one or four pulses are input from this pin for each revolution of the disc motor. It controls the AFC and APO output so that the disc motor rpms are within 175 ~ 740 rpms.
<table><tr><th>Disc motor revolutions (rpm)</th><th>AFCO</th><th>APC</th></tr><tr><td>~ 175</td><td>"H" level fixed</td><td>Duty cycle 50% output fixed</td></tr><tr><td>175 ~ 740</td><td>Normal operation</td><td>Normal operation</td></tr><tr><td>740 ~</td><td>"L" level fixed</td><td>Duty cycle 50% output fixed</td></tr></table></td></tr>
<tr><td>15</td><td>4/1</td><td>Input</td><td>This pin selects either one or four pulses for each revolution of the disc motor, set by the FGIN input pulse.
<table><tr><th>FG pulse</th><th>4/1</th></tr><tr><td>1</td><td>"H" level</td></tr><tr><td>4</td><td>"L" level</td></tr></table></td></tr>
<tr><td>16</td><td>OVRG</td><td>Input</td><td>This pin decides whether or not to control the disc motor revolutions with FGIN input.
The FGIN input becomes active at "H" level</td></tr>
<tr><td>17</td><td>APCG</td><td>Input</td><td>ON/OFF switch for the generator which generates CLV servo control APC signals.
It turns OFF at "L" level and ON at "H" level.</td></tr>
<tr><td>18</td><td>DMLD</td><td>Output</td><td>Lock detection output pin located on the CLV servo control AFC signal generator. "H" level when the lock.</td></tr>
<tr><td>19</td><td>APCO</td><td>Output</td><td>CLV servo control APC signal output pin.</td></tr>
<tr><td>20</td><td>AFCO</td><td>Output</td><td>CLV servo control AFC signal output pin.</td></tr>
<tr><td>21</td><td>P/S̄</td><td>Input</td><td>CLV servo control signal ON/OFF switch.
"H" level while playing, "L" level while being stopped.</td></tr>
<tr><td>22</td><td>SCSE</td><td>Input</td><td>For selecting data for sub-code signal output pins SCP/T to S/W4.
Each outputs four-bit data. At "L" level, P, Q, R and S; and at "H" level, T, U, V and W.</td></tr>
<tr><td>23</td><td>SCPT</td><td>Output</td><td rowspan="4">Sub-code signal P, Q, R, S, T, U, V, W, eight-bits data output pin.
This signal is data for each frame and is always output in four-bit units by the SCSE signal.</td></tr>
<tr><td>24</td><td>SCQU</td><td>Output</td></tr>
<tr><td>25</td><td>SCRV</td><td>Output</td></tr>
<tr><td>26</td><td>SCSW</td><td>Output</td></tr>
<tr><td>27, 61</td><td>VDD</td><td></td><td>Voltage supply (+5 V)</td></tr>
<tr><td>28</td><td>VSS</td><td></td><td>GND</td></tr>
<tr><td>29</td><td>SOS I</td><td>Output</td><td>This pin becomes "H" level when either sub-code synchronized pattern SO or SI is detected, for duration of that input frame period.</td></tr>
<tr><td>30</td><td>N. C</td><td></td><td></td></tr>
<tr><td>31</td><td>PFCK</td><td>Output</td><td>The frame period duty cycle is approx 50% output.
The sub-code data changes to synchronize with the output trailing edge.</td></tr>
<tr><td>32</td><td>QDSS</td><td>Input</td><td>This pin selects the sub-code synchronized pattern detection mode which is used in demodulating the sub-code signal Q.</td></tr>
<tr><td>33
∫
36</td><td>N. C
∫
N. C</td><td></td><td></td></tr>
<tr><td>37</td><td>QDAS</td><td>Input</td><td>This pin switches the data of the sub-code signal Q data output pin. Fixed to "L" level.</td></tr>
<tr><td>38
∫
41</td><td>N. C
∫
N. C</td><td></td><td></td></tr>
</table>

<table>
<tr><th>Pin</th><th>Pin name</th><th>I/O</th><th>Function</th></tr>
<tr><td>42</td><td>WSEG</td><td>Input</td><td>This signal is a gate signal window selection pin that determines whether or not to give out an internal synchronized signal when an EFM signal frame synchronize pattern has been detected.<table><tr><th>WSEG</th><th>Gate signal window (PLCK clock number)</th></tr><tr><td>L</td><td>± 3</td></tr><tr><td>H</td><td>± 7</td></tr></table></td></tr>
<tr><td>43</td><td>TMWS</td><td>Input</td><td><table><tr><th>TMWS</th><th>N(PLCK)</th></tr><tr><td>H</td><td>11 ± 0.5</td></tr></table></td></tr>
<tr><td>44</td><td>ESGM</td><td>Input</td><td rowspan="2"><table><tr><th>ESGL</th><th>ESGM</th><th>N(Frame)</th></tr><tr><td>H</td><td>H</td><td>2</td></tr></table></td></tr>
<tr><td>45</td><td>ESGL</td><td>Input</td></tr>
<tr><td>46</td><td>TMGS</td><td></td><td><table><tr><th>TMGS</th><th>N</th></tr><tr><td>L</td><td>7</td></tr></table></td></tr>
<tr><td>47</td><td>N. C</td><td></td><td></td></tr>
<tr><td>48</td><td>TMO</td><td>Output</td><td>This pin outputs, in three states, the result of comparison between the maximum cycle (Tmax) of the DEFM signal and the PLCK frequency.
When "L," f (DEFM) 〈 f (PLCK). When "H," f (DEFM) 〉 F (PLCK).
The P/$\overline{S}$ signal at "L" forces TMO to become fixed at the "H" level.</td></tr>
<tr><td>49</td><td>QDSE</td><td>Input</td><td>Effective use of the micro computer input port can be made with this pin.
It becomes high impedance at the "L" level.</td></tr>
<tr><td>50</td><td>TMOE</td><td>Input</td><td>Forces TMO output to becomes high impedance. It becomes high impedance at the "L" level.</td></tr>
<tr><td>51</td><td>FSPS</td><td>Output</td><td>Displays the system synchronization state with the frame synchronize pattern.</td></tr>
<tr><td>52</td><td>DEFM</td><td>Input</td><td>This is the input pin for the EFM signal reproduced from the disc.
The signal from the RF amplifier is sliced by the level comparator and input directly (asynchronous with PLCK) to this pin.</td></tr>
<tr><td>53</td><td>EFMI</td><td>Input</td><td>Input pin for the EFM signal reproduced from the disc.
Inputs a signal synchronized with the PLCK leading edge which is phase-locked by the PLL circuit.</td></tr>
<tr><td>54</td><td>PLCK</td><td>Input</td><td>Input pin for the clock pulse for separating the frame synchronisation signal and data. The clock pulse generated by an external PLL circuit using the HF signal reproduced from the disc.
System lock: 4.3218 MHz, Duty cycle = 50%.</td></tr>
<tr><td>55</td><td>FSLO</td><td>Output</td><td>Not in use.</td></tr>
<tr><td>56</td><td>PBFS</td><td>Output</td><td>When each frame period signal is "H" level, the demodulated data UO to U31 are transferred to TC9179F
The first MWRE signal that has been output after this pin becomes "H" level indicates that symbol UO can be output.</td></tr>
<tr><td>57
≀
60
•
62
≀
65</td><td>DB0
≀
DB3
•
DB4
≀
DB7</td><td>Output
Output
Output
Output</td><td>Pins for outputting the demodulated data (UO to U31) for each frame.
This is a three-state output. When the BOEN input is "L" level, data is output.</td></tr>
<tr><td>66</td><td>BOEN</td><td>Input</td><td>This is an enable signal input pin which turns on DB0 to DB7 (bus driver) .</td></tr>
<tr><td>67</td><td>MWRE</td><td>Output</td><td>This signal output pin indicates whether or not it is possible to write DB0 to DB7 output into the external RAM.</td></tr>
</table>

*IC5 : HM6116ASP-20


Vcc
A7
A6
R/$\overline{W}$
$\overline{OE}$
A2
$\overline{CS}$
DB7
DB6
DB5
DB4
DB3
24
23
22
21
20
19
18
17
16
15
14
13
MEMORY MATRIX 128 x 128
ROW DECODER
COLUMN I/O
COLUMN DECODER
INPUT DATA CONTROL
1
2
3
4
5
6
7
8
9
10
11
12
A10
A9
A8
A5
A4
A3
A1
A0
DB2
DB1
DB0
GND

* IC6 : TC9179F

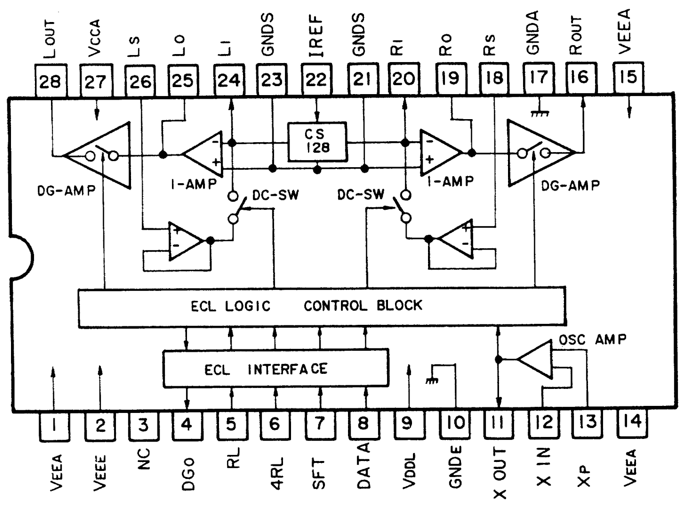

CKSE
X-I
X-O
L/RG
$\overline{WDCK}$
MLCK
BCK
SDATA
DA-6(AP-L)
DA-5(AP-R)
DA-4(CKIM)
DA-3(HOF-LL)
NC
NC
DA-2 (HOF-L)
DA-1 (HOF-M)
DA-0 (SD-OL)
$\overline{P/S}$ SE
MUT-02
MUT-01
MUT-1
$\overline{ATT-3}$
54
53
52
51
50
49
48
47
46
45
44
43
42
41
40
39
38
37
36
35
34
33
CK4M 55
CK2M 56
TES1 57
TES2 58
COFS 59
DSLP 60
VDD 61
Vss 62
DAST 63
DIV- 64
DIV+ 65
BUSE 66
Vss 67
Timing generator circuit
Test circuit
Data status output circuit
RAM address signal generator R/W control circuit
Data output circuit
Attenuator circuit
Muting circuit
Data correction circuit
Micro program ROM
Arithmetic and logic circuit
C1, C2 error detection correction circuit
32 $\overline{ATT-2}$
31 $\overline{ATT-1}$
30 $\overline{ATT-0}$
29 ALGC
28 Vss
27 VDD
26 DB0
25 DB1
24 DB2
23 DB3
22 DB4
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
NC
PBFS
MWRE
BOEN
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
R/$\overline{W}$
CE2
CE1
A10
DB7
DB6
DB5

TC9179F Pin Function Description

CD system DAD error detection correction signal processor LSI

Pin	Pin name	I/O	Function
1	N. C		
2	PBFS	Input	Frame synchronized input.
3	MWRE	Input	Memory write request input.
4	BOEN	Output	Output enable pin. This is a control signal output pin that enables the symbol data output pins (DB0 to DB7) when it has become possible to receive the MWRE signal from TC9179F.
5 ≀ 14	A0 ≀ A9	Output Output	RAM address signal. External RAM (eight bits x 2 kW) address control signal output.
18	A10	Output	
15	R/$\overline{W}$	Output	Read/write signal pin. Controls the external read/write. Read at "H" level, Write at "L" level.
16	CE2	Output	Chip enable pin, Becomes "H" when correction data is written into an external RAM during C2 correction. (Not in use.)
17	CE1	I/O	Chip enable pin for reading/writing external RAM.
19 ≀ 26	DB7 ≀ DB0	I/O	Data bus line. I/O pin which sends data to the external RAM or TC9178F.
27,	VDD		Power supply (+5 V)
28 • 62 • 67	VSS VSS VSS		GND

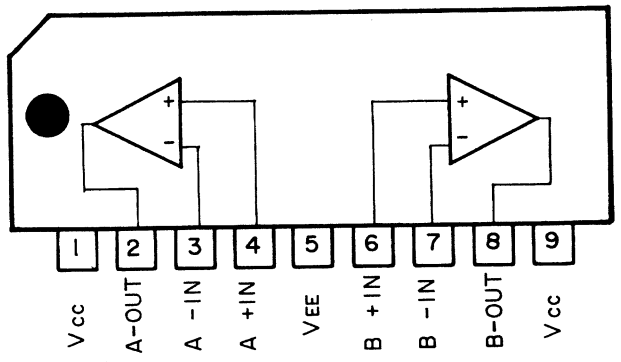
IC12 : TD6705AP


L OUT
VCCA
Ls
Lo
LI
GNDS
IREF
GNDS
RI
Ro
Rs
GNDA
ROUT
VEEA
28
27
26
25
24
23
22
21
20
19
18
17
16
15
CS 128
DG-AMP
I-AMP
DC-SW
DC-SW
I-AMP
DG-AMP
ECL LOGIC CONTROL BLOCK
ECL INTERFACE
OSC AMP
1
2
3
4
5
6
7
8
9
10
11
12
13
14
VEEA
VEEE
NC
DGo
RL
4RL
SFT
DATA
VDDL
GNDE
X OUT
X IN
XP
VEEA

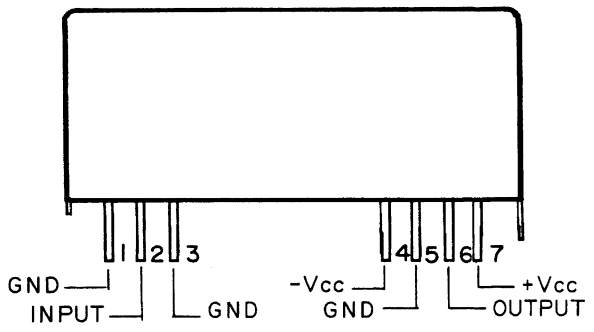
TD6705AP Pin Functions

Pin	Pin name	I/O	Function
1	VEEA		Analog power supply (−9 V).
14	VEEA		
15	VEEA		
2	VEEE		Digital power supply (−5 V).
3	N. C		Digital GND
4	DGO		Not in use
5	RL	Input	Input data L, R cnannels indicator signal input. (44.1 kHz) Duty cycle = 50%. The "L" level is Lch, and the "H" level is Rch, and is used as a control signal within the LSI.
6	4RL	Input	This input pin quadruples the RL (44.1KHz) frequency. (176.4 kHz) Duty cycle = 50%. Used as a control signal within the LSI.
7	SFT	Input	This is a shift clock input pin which reads the PCM digital audio data in 16 bits units from the MSB side bit serial, into the LSI. (1.4112 MHz) Duty cucle = 50%.
8	DATA	Input	PCM digital audio data input. Inputs from MSB in 16-bits units in bit serial.
9	VCC		Digital voltage supply. (+5 V)
10	GNDE		Digital GND
11	X OUT	Output	Generator circuit I/O pin. By joining L, C, and R, it makes up a modified Colpitts oscillator circuit.
12	X IN	Input	
13	X P		
16	R OUT	Output	Internal Deglitcher amplifier output pin. (Rch and Lch) It outputs the Rch and Lch integrator hold voltage by means of a 44.1kHz, PAM wave with a dury cycle of 50%.
28	L OUT	Output	
17	GNDA		Analog GND.
18	RS	Input	This is a discharge amplifier input pin inside the LSI. (Rch and Lch)
26	LS	Input	
19	RO	Input	Deglicher amplifier input pin (Operational amplifier output point)
25	LO	Input	
20	RI	Input	Operational amplifier inverted (—) input pin. This pin is also used to connect a constant current source and an analogue switch.
24	LI	Input	Current source and built-in analogue switch. (Rch and Lch)
21	GNDS		Analogue GND.
23	GNDS		
22	IREF	Input	Standard current input pin for setting a constant current.
27	VCC		Analogue voltage supply. (+8V)

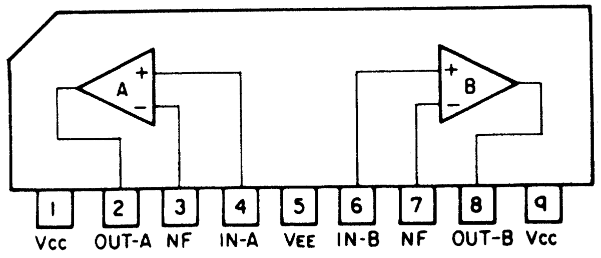
IC13 : NJM072S


+
−
+
−
1
2
3
4
5
6
7
8
9
Vcc
A-OUT
A −IN
A +IN
VEE
B +IN
B −IN
B-OUT
Vcc

IC14, IC15, CWW-225

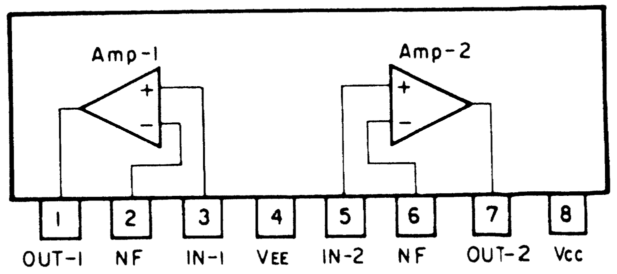

1
2
3
4
5
6
7
GND
INPUT
GND
-Vcc
GND
+Vcc
OUTPUT

IC16, IC17 : TA75558S

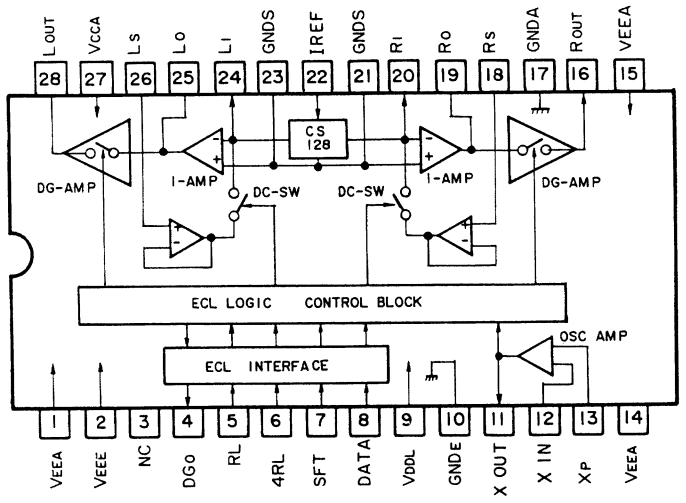

A
+
−
B
+
−
1
2
3
4
5
6
7
8
9
Vcc
OUT-A
NF
IN-A
VEE
IN-B
NF
OUT-B
Vcc

- **Pre Amp Assy**

IC1: M5218L


Amp-1
Amp-2
+
−
+
−
1
2
3
4
5
6
7
8
OUT-1
NF
IN-1
VEE
IN-2
NF
OUT-2
Vcc

IC12 : TD6705AP

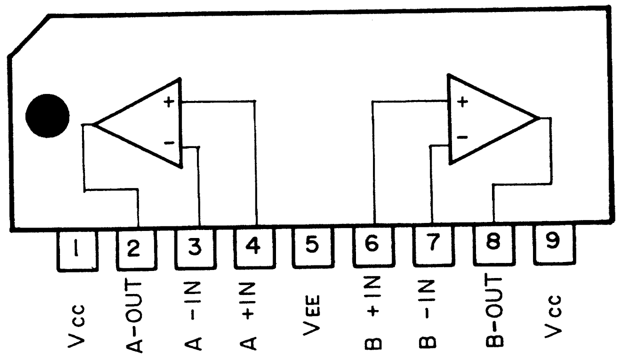

L OUT
VCCA
LS
Lo
LI
GNDS
IREF
GNDS
RI
Ro
Rs
GNDA
ROUT
VEEA
28
27
26
25
24
23
22
21
20
19
18
17
16
15
DG-AMP
I-AMP
CS 128
DC-SW
DC-SW
I-AMP
DG-AMP
ECL LOGIC CONTROL BLOCK
ECL INTERFACE
OSC AMP
1
2
3
4
5
6
7
8
9
10
11
12
13
14
VEEA
VEEE
NC
DGO
RL
4RL
SFT
DATA
VDDL
GNDE
X OUT
X IN
XP
VEEA

TD6705AP Pin Functions

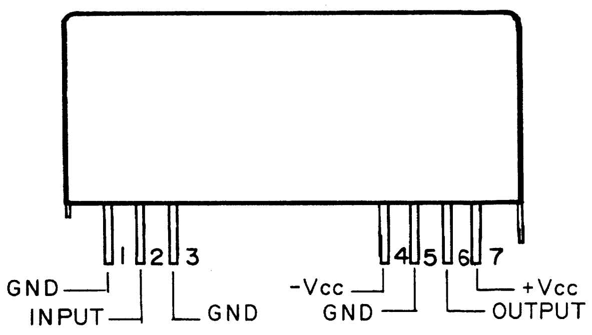
Pin	Pin name	I/O	Function
1	VEEA		Analog power supply (−9 V).
14	VEEA		
15	VEEA		
2	VEEE		Digital power supply (−5 V).
3	N. C		Digital GND
4	DGO		Not in use
5	RL	Input	Input data L, R cnannels indicator signal input. (44.1 kHz) Duty cycle = 50%. The "L" level is Lch, and the "H" level is Rch, and is used as a control signal within the LSI.
6	4RL	Input	This input pin quadruples the RL (44.1KHz) frequency. (176.4 kHz) Duty cycle = 50%. Used as a control signal within the LSI.
7	SFT	Input	This is a shift clock input pin which reads the PCM digital audio data in 16 bits units from the MSB side bit serial, into the LSI. (1.4112 MHz) Duty cucle = 50%.
8	DATA	Input	PCM digital audio data input. Inputs from MSB in 16-bits units in bit serial.
9	VCC		Digital voltage supply. (+5 V)
10	GNDE		Digital GND
11	X OUT	Output	Generator circuit I/O pin. By joining L, C, and R, it makes up a modified Colpitts oscillator circuit.
12	X IN	Input	
13	X P		
16	R OUT	Output	Internal Deglitcher amplifier output pin. (Rch and Lch) It outputs the Rch and Lch integrator hold voltage by means of a 44.1kHz, PAM wave with a dury cycle of 50%.
28	L OUT	Output	
17	GNDA		Analog GND.
18	RS	Input	This is a discharge amplifier input pin inside the LSI. (Rch and Lch)
26	LS	Input	

Pin	Pin name	I/O	Function
19	RO	Input	Deglicher amplifier input pin (Operational amplifier output point)
25	LO	Input	
20	RI	Input	Operational amplifier inverted (−) input pin. This pin is also used to connect a constant current source and an analogue switch.
24	LI	Input	Current source and built-in analogue switch. (Rch and Lch)
21	GNDS		Analogue GND.
23	GNDS		
22	IREF	Input	Standard current input pin for setting a constant current.
27	VCC		Analogue voltage supply. (+8V)

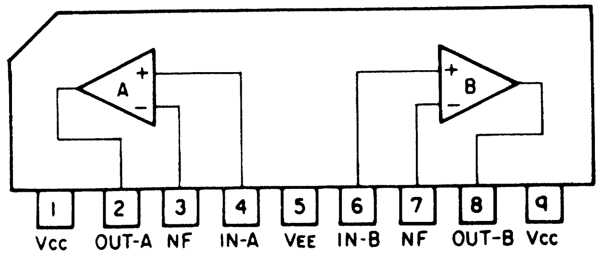
IC13 : NJM072S


1
2
3
4
5
6
7
8
9
Vcc
A-OUT
A −IN
A +IN
VEE
B +IN
B −IN
B-OUT
Vcc

IC14, IC15, CWW-225

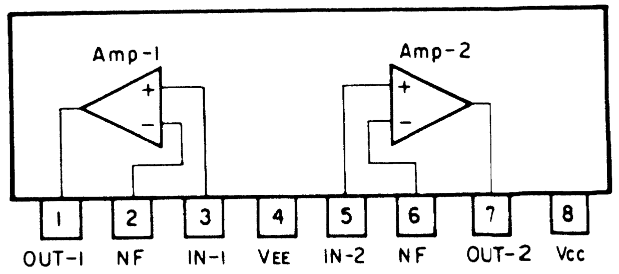

1
2
3
4
5
6
7
GND
INPUT
GND
−Vcc
GND
+Vcc
OUTPUT

IC16, IC17 : TA75558S


A
B
1
2
3
4
5
6
7
8
9
Vcc
OUT-A
NF
IN-A
VEE
IN-B
NF
OUT-B
Vcc

- **Pre Amp Assy**

IC1: M5218L


Amp-1
Amp-2
1
2
3
4
5
6
7
8
OUT-1
NF
IN-1
VEE
IN-2
NF
OUT-2
Vcc

11. SCHEMATIC DIAGRAM & P.C. BOARD PATTERNS

11.1 OVERALL CONNECTIONS DIAGRAM

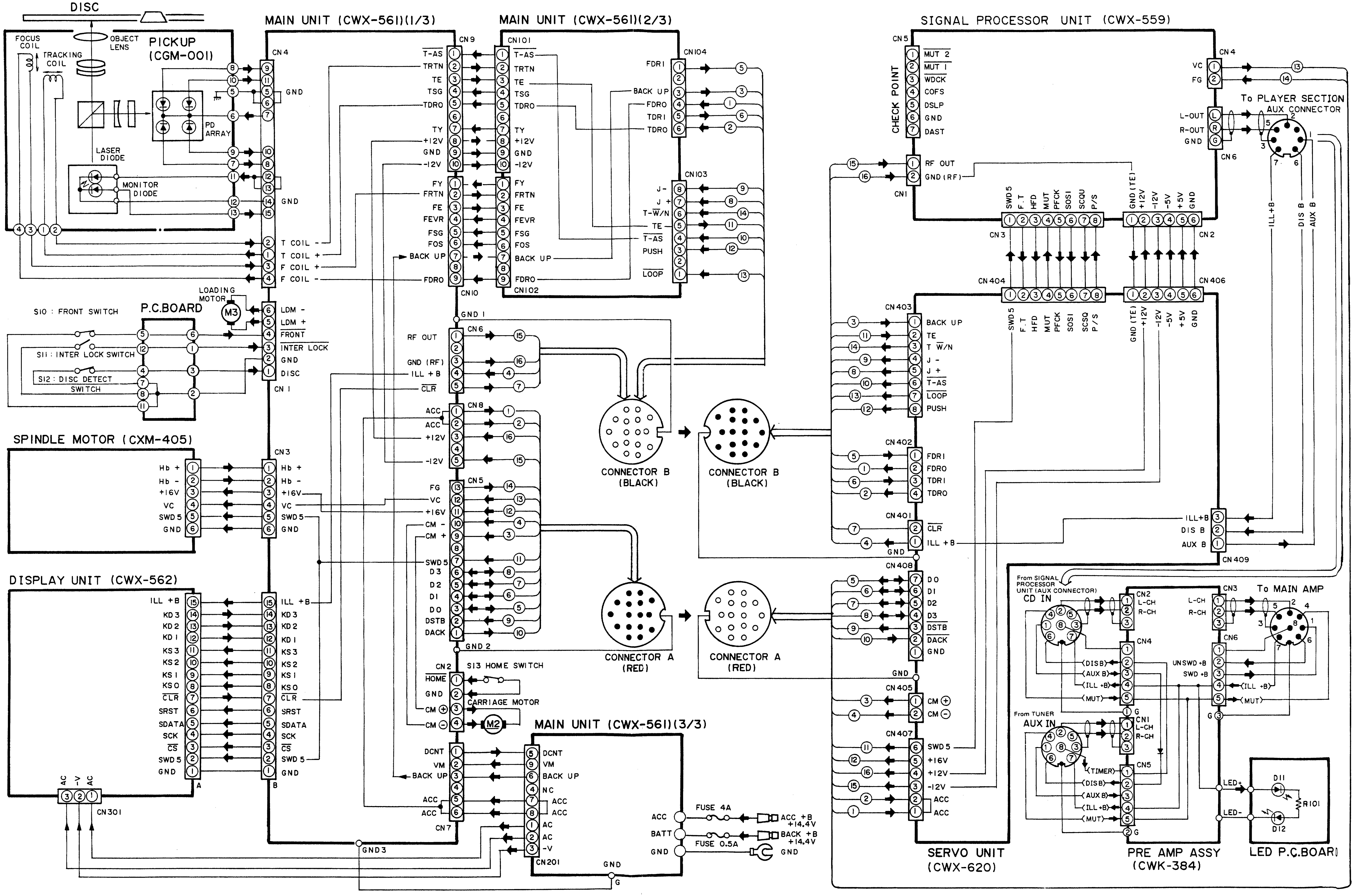

DISC
FOCUS COIL
TRACKING COIL
OBJECT LENS
PICKUP (CGM-001)
PD ARRAY
LASER DIODE
MONITOR DIODE
MAIN UNIT (CWX-561)(1/3)
MAIN UNIT (CWX-561)(2/3)
MAIN UNIT (CWX-561)(3/3)
SIGNAL PROCESSOR UNIT (CWX-559)
CHECK POINT
MUT 2
MUT 1
WDCK
COFS
DSLP
GND
DAST
RF OUT
GND (RF)
VC
FG
L-OUT
R-OUT
To PLAYER SECTION AUX CONNECTOR
ILL+B
DIS B
AUX B
SWD5
F.T
HFD
MUT
PFCK
SOSI
SCSQ
P/S
GND (TE)
+12V
-12V
-5V
+5V
CN4
CN9
CN101
CN104
CN103
CN10
CN102
CN5
CN1
CN6
CN3
CN2
CN404
CN406
CN403
CN402
CN401
CN409
CN408
CN405
CN407
CN8
CN7
CN201
CN301
T-AS
TRTN
TE
TSG
TDRO
TY
FY
FRTN
FE
FEVR
FSG
FOS
BACK UP
FDRO
FDRI
TDRI
J-
J+
T-W/N
PUSH
LOOP
T COIL -
T COIL +
F COIL +
F COIL -
LOADING MOTOR
M3
P.C.BOARD
S10 : FRONT SWITCH
S11 : INTER LOCK SWITCH
S12 : DISC DETECT SWITCH
LDM -
LDM +
FRONT
INTER LOCK
DISC
GND 1
GND 2
GND 3
ILL +B
CLR
ACC
SPINDLE MOTOR (CXM-405)
Hb +
Hb -
+16V
VC
CM -
CM +
D3
D2
D1
D0
DSTB
DACK
DISPLAY UNIT (CWX-562)
KD3
KD2
KD1
KS3
KS2
KS1
KS0
SRST
SDATA
SCK
CS
AC
-V
CONNECTOR B (BLACK)
CONNECTOR A (RED)
CN2 S13 HOME SWITCH
HOME
CARRIAGE MOTOR
M2
DCNT
VM
NC
FUSE 4A
FUSE 0.5A
ACC +B +14.4V
BACK +B +14.4V
BATT
SERVO UNIT (CWX-620)
From SIGNAL PROCESSOR UNIT (AUX CONNECTOR) CD IN
From TUNER AUX IN
L-CH
R-CH
To MAIN AMP
UNSWD +B
SWD +B
TIMER
DISB
AUX B
PRE AMP ASSY (CWK-384)
LED+
LED-
D11
D12
R101
LED P.C.BOARD
1
2
3
4
5
6
A
B
C
D

Fig. 61

- Connector Line Waveforms

Photo 1 COFS
H : 50μs/div
V : 0.1V/div

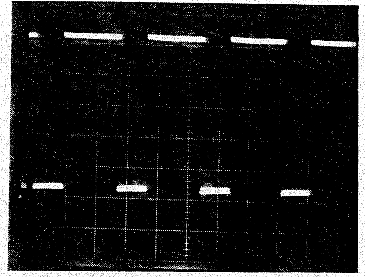


Photo 2 CS
H : 10ms/div
V : 0.1V/div

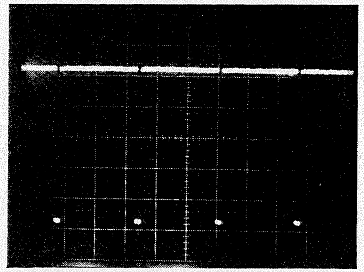


Photo 3 D0~D3
H : 1ms/div
V : 0.1V/div

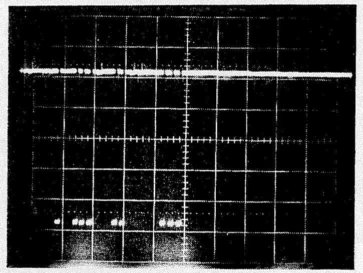


Photo 4 DACK
DSTB
H : 1ms/div
V : 0.1V/div

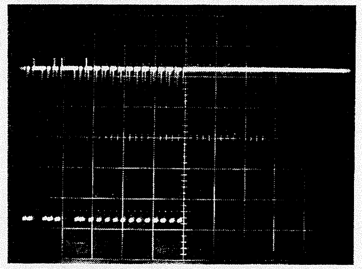


Photo 5 DAST
H : 50μs/div
V : 0.1V/div

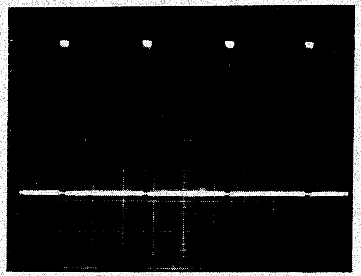


Photo 6 DSLP
H : 50μs/div
V : 0.1V/div

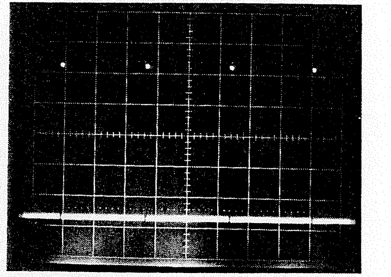


Photo 7 FDRI
H : 0.5ms/div
V : 50ms/div

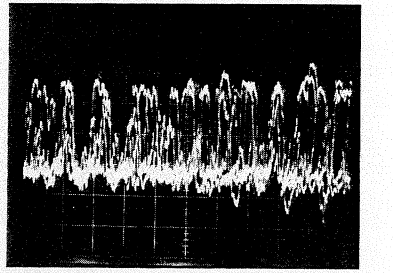


Photo 8 FDRO
H : 0.2ms/div
V : 50mV/div

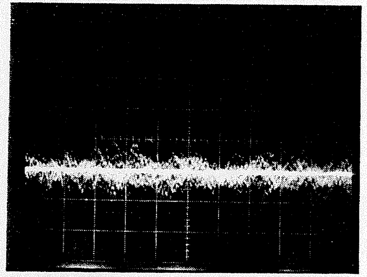


Photo 9 FE
H : 1ms/div
V : 10mV/div

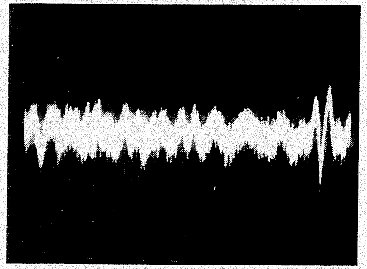


Photo 10 FG
H : 10ms/div
V : 0.1V/div

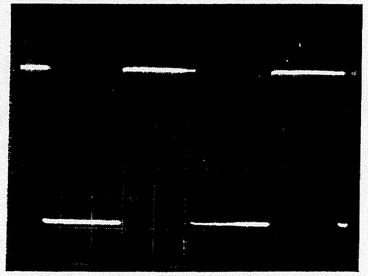


Photo 11 KD1~KD3
KS0~KS3
H : 2ms/div
V : 0.1V/div

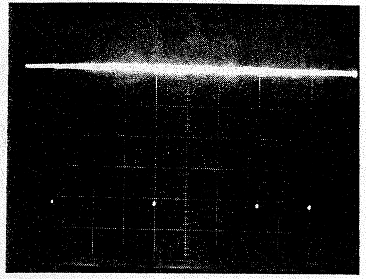


Photo 12 PFCK
H : 50μs/div
V : 0.1V/div

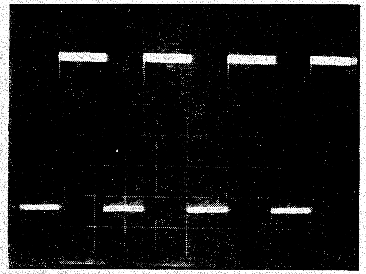


Photo 13 RF OUT
H : 0.5μs/div
V : 50ms/div

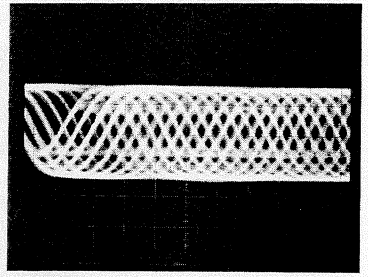


Photo 14 SOSI
H : 5ms/div
V : 0.1V/div

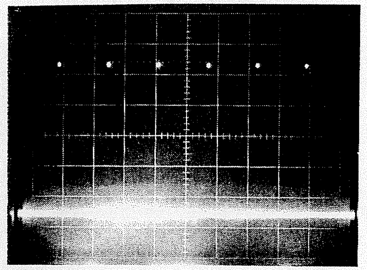


Photo 15 SCQU
H : 0.1μs/div
V : 0.1V/div

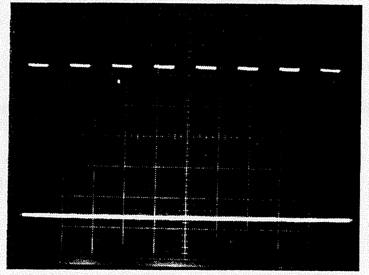


Photo 16 TDRI
H : 1ms/div
V : 50ms/div

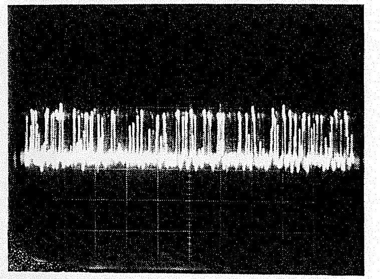


Photo 17 TDRO
H : 0.2ms/div
V : 50ms/div

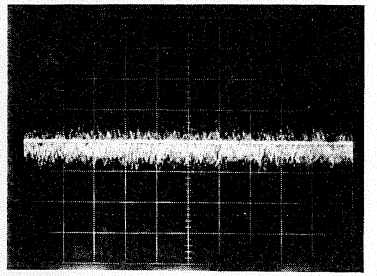


Photo 18 TE
H : 0.5ms/div
V : 50mV/div

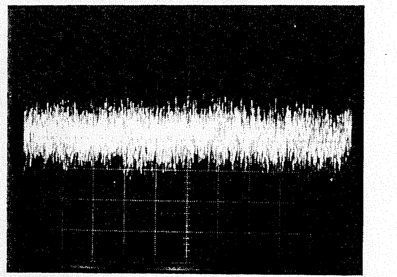
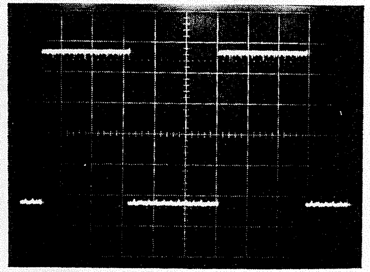


Photo 19 WDCK
H : 2μs/div
V : 0.1V/div



Note:
These waveforms were photographed during the PLAY operation and are reference values. They were measured using the 10:1 probe of the oscilloscope.

Photo 11 KD1~KD3 KS0~KS3 [H : 2ms/div V : 0.1V/div]

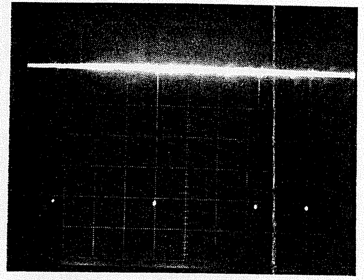


Photo 12 PFCK [H : 50μs/div V : 0.1V/div]

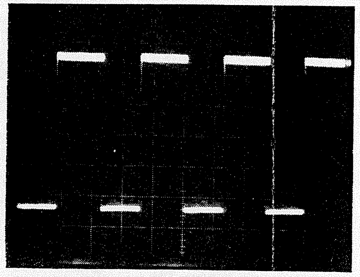


Photo 13 RF OUT [H : 0.5μs/div V : 50ms/div]

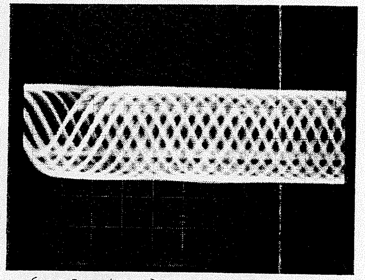


Photo 14 SOSI [H : 5ms/div V : 0.1V/div]

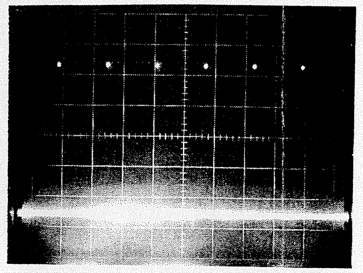


Photo 15 SCQU [H : 0.1μs/div V : 0.1V/div]

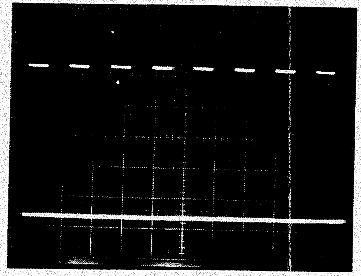


Photo 16 TDRI [H : 1ms/div V : 50ms/div]

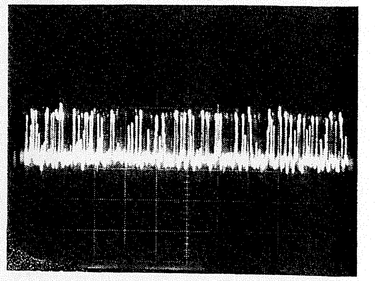


Photo 17 TDRO [H : 0.2ms/div V : 50ms/div]

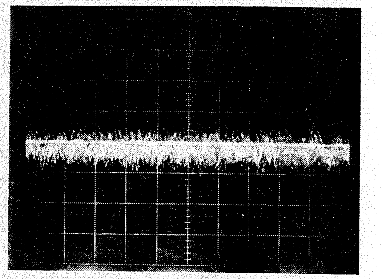


Photo 18 TE [H : 0.5ms/div V : 50mV/div]

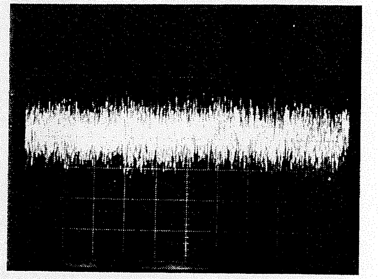
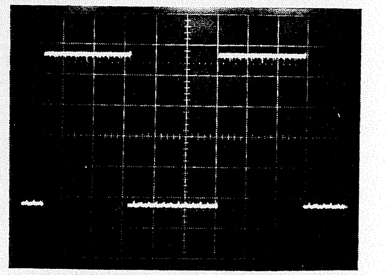
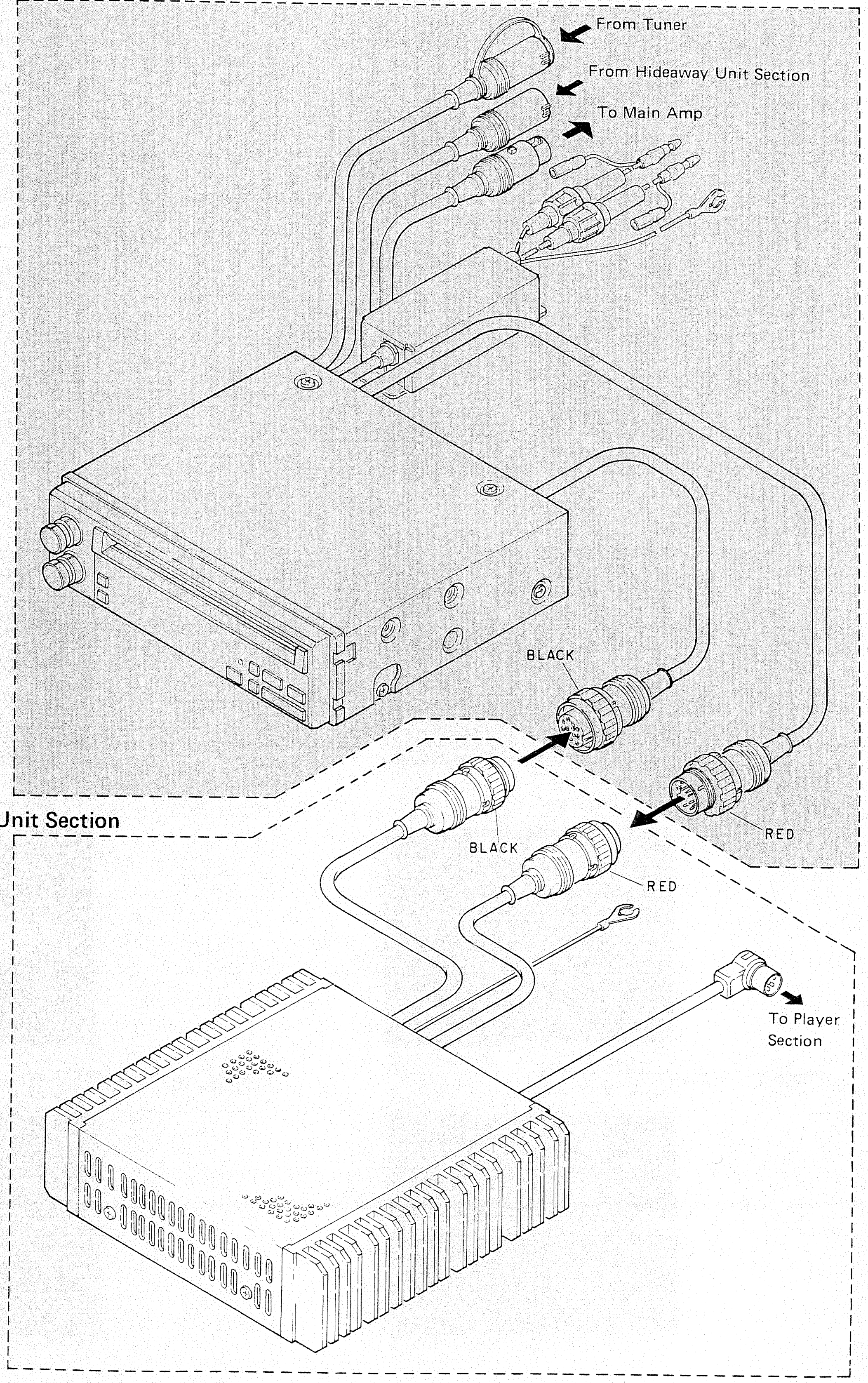


Photo 19 WDCK [H : 2μs/div V : 0.1V/div]



Note:
These waveforms were photographed during the PLAY operation and are reference values. They were measured using the 10:1 probe of the oscilloscope.

- The circuit diagram shown in Fig. 64 and 72 represent the circuits in the shaded area.
- Player Section

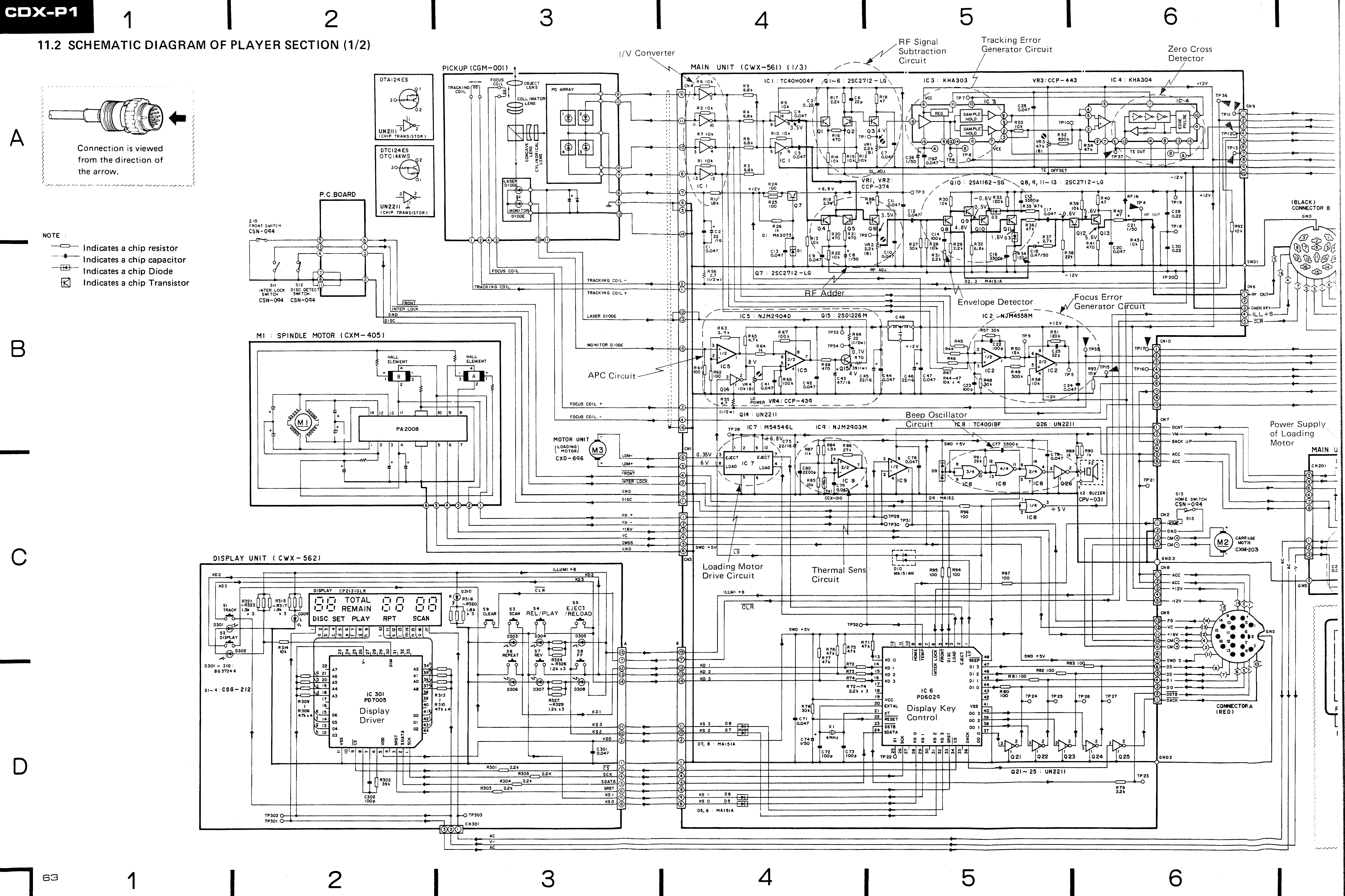

From Tuner
From Hideaway Unit Section
To Main Amp
BLACK
RED
BLACK
RED
To Player Section

- Hideaway Unit Section

Fig. 62

Fig. 63

11.2 SCHEMATIC DIAGRAM OF PLAYER SECTION (1/2)


1
2
3
4
5
6
A
B
C
D
Connection is viewed from the direction of the arrow.
NOTE :
Indicates a chip resistor
Indicates a chip capacitor
Indicates a chip Diode
Indicates a chip Transistor
DTA124ES
UN2111 (CHIP TRANSISTOR)
DTC124ES
DTC144WS
UN2211 (CHIP TRANSISTOR)
PICKUP (CGM-001)
TRACKING COIL
FOCUS COIL
OBJECT LENS
COLLIMATOR LENS
CONCAVE LENS
CYLINDRICAL LENS
PD ARRAY
LASER DIODE
MONITOR DIODE
P.C.BOARD
S10 FRONT SWITCH CSN-094
S11 INTER LOCK SWITCH CSN-094
S12 DISC DETECT SWITCH CSN-094
M1 : SPINDLE MOTOR (CXM-405)
HALL ELEMENT
PA2008
MOTOR UNIT (LOADING MOTOR) CXD-696
M3
I/V Converter
RF Signal Subtraction Circuit
Tracking Error Generator Circuit
Zero Cross Detector
MAIN UNIT (CWX-561) (1/3)
IC1 : TC40H004F
Q1~6 : 2SC2712-LG
IC3 : KHA303
VR3 : CCP-443
IC4 : KHA304
SAMPLE HOLD
EDGE PULSE
TE OFFSET
TE OUT
VR1, VR2 : CCP-374
Q10 : 2SA1162-SG
Q8, 9, 11~13 : 2SC2712-LG
Q7 : 2SC2712-LG
RF Adder
Envelope Detector
D2, 3 : MA151A
RF ADJ
DL ADJ
Focus Error Generator Circuit
IC5 : NJM2904D
Q15 : 2SD1226M
IC2 : NJM4558M
APC Circuit
LD POWER VR4 : CCP-439
Q14 : UN2211
IC7 : M54546L
IC9 : NJM2903M
Beep Oscillator Circuit
IC8 : TC4001BF
Q26 : UN2211
X2 BUZZER CPV-031
Loading Motor Drive Circuit
Thermal Sens Circuit
TH1 CCX-010
D9 : MA153
D10 MA151WK
(BLACK) CONNECTOR B
Power Supply of Loading Motor
MAIN U
S13 HOME SWITCH CSN-094
M2 CARRIAGE MOTOR CXM-203
CONNECTOR A (RED)
IC6 PD6029 Display Key Control
Q21~25 : UN2211
D7, 8 : MA151A
D5, 6 : MA151A
DISPLAY UNIT (CWX-562)
DISPLAY CP2131GLR
TOTAL REMAIN
DISC SET PLAY RPT SCAN
S1 TRACK
S2 DISPLAY
S3 SCAN
S4 REL/PLAY
S5 EJECT /RELOAD
S6 REPEAT
S7 REV
S8 FF
S9 CLEAR
D301 ~ 310 : 8G 5724 K
S1~4 : CSG-212
IC 301 PD7005 Display Driver
CN301
TP301
TP302
TP303

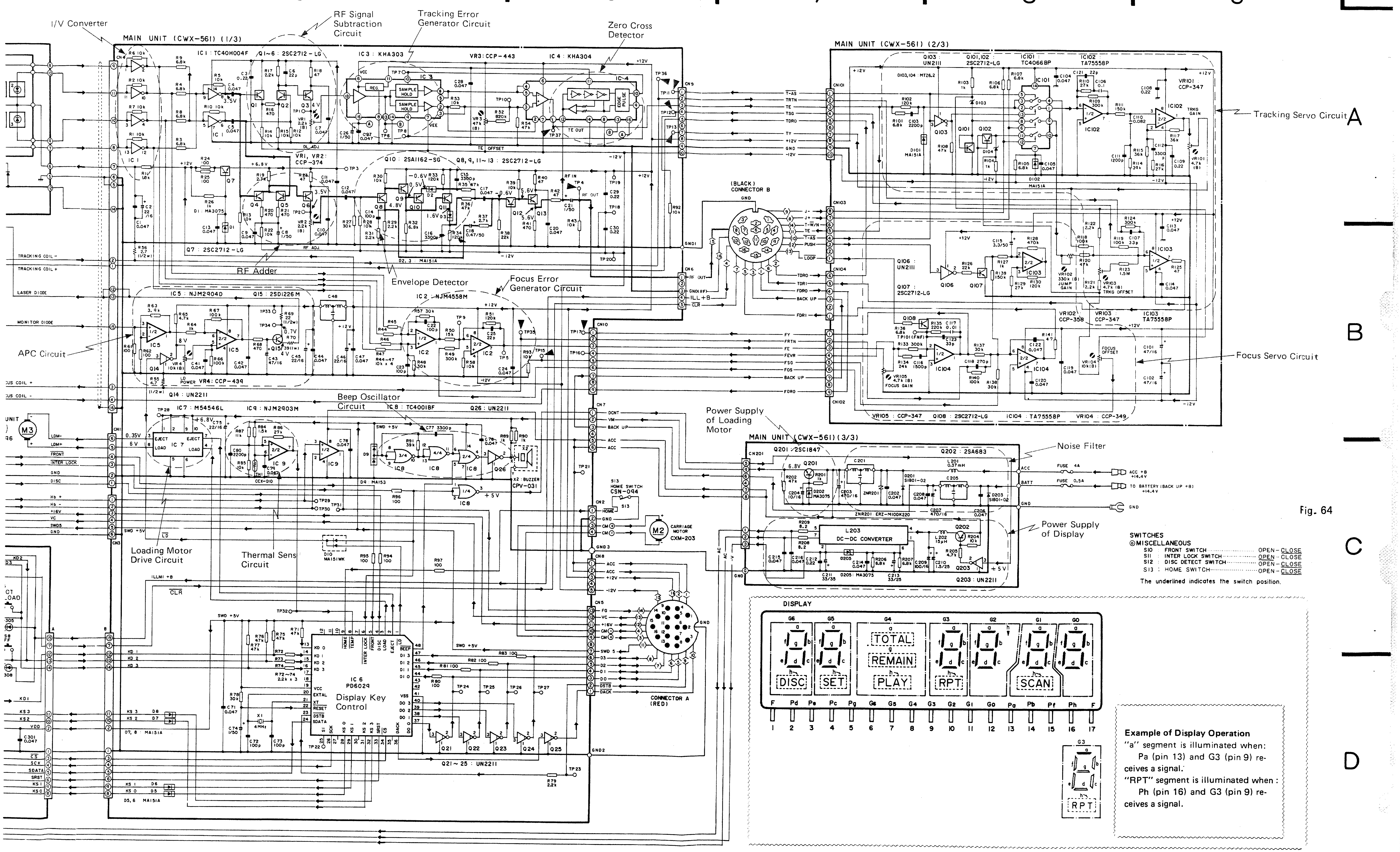

4
5
6
7
8
9
A
B
C
D
I/V Converter
RF Signal Subtraction Circuit
Tracking Error Generator Circuit
Zero Cross Detector
MAIN UNIT (CWX-561) (1/3)
IC1 : TC40H004F
Q1~6 : 2SC2712-LG
IC3 : KHA303
VR3 : CCP-443
IC4 : KHA304
SAMPLE HOLD
EDGE PULSE
TE OFFSET
TE OUT
DL ADJ
VR1, VR2: CCP-374
Q10 : 2SA1162-SG
Q8, 9, 11~13 : 2SC2712-LG
RF IN
RF OUT
RF ADJ
D2, 3 : MA151A
Q7 : 2SC2712-LG
RF Adder
Envelope Detector
Focus Error Generator Circuit
TRACKING COIL −
TRACKING COIL +
LASER DIODE
MONITOR DIODE
IC5 : NJM2904D
Q15 : 2SD1226M
IC2 : NJM4558M
APC Circuit
VR4 : CCP-434
Q14 : UN2211
Beep Oscillator Circuit
IC7 : M54546L
IC9 : NJM2903M
IC8 : TC4001BF
Q26 : UN2211
EJECT
LOAD
X2 : BUZZER CPV-031
CCX-010
D9 : MA153
Loading Motor Drive Circuit
Thermal Sens Circuit
D10 MA151WK
M3
M2
CARRIAGE MOTOR CXM-203
S13 HOME SWITCH CSN-094
IC 6 PD6029 Display Key Control
Q21~25 : UN2211
D7, 8 : MA151A
D5, 6 : MA151A
CONNECTOR A (RED)
(BLACK) CONNECTOR B
MAIN UNIT (CWX-561) (2/3)
Q103 UN2111
Q101, 102 2SC2712-LG
IC101 TC4066BP
IC102 TA75558P
D103, 104 : MTZ6.2
D101 MA151A
D102 MA151A
VR101 CCP-347
TRKG GAIN
Tracking Servo Circuit
Q106 UN2111
Q107 2SC2712-LG
IC103 TA75558P
VR102 CCP-358
VR103 CCP-347
JUMP GAIN
TRKG OFFSET
FOCUS OFFSET
FOCUS GAIN
IC104
Focus Servo Circuit
VR105 : CCP-347
Q108 : 2SC2712-LG
IC104 : TA75558P
VR104 : CCP-349
Power Supply of Loading Motor
MAIN UNIT (CWX-561) (3/3)
Q201 : 2SC1847
Q202 : 2SA683
Noise Filter
D202 MA3075
ZNR201 : ERZ-M10DK220
L203 DC-DC CONVERTER
Q203 : UN2211
D205 : MA3075
Power Supply of Display
FUSE 4A
FUSE 0.5A
ACC +B +14.4V
TO BATTERY (BACK UP +B) +14.4V
GND
DISPLAY
TOTAL
REMAIN
PLAY
DISC
SET
RPT
SCAN
G6
G5
G4
G3
G2
G1
G0
F Pd Pe Pc Pg G6 G5 G4 G3 G2 G1 G0 Pa Pb Pf Ph F
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17

Fig. 64

SWITCHES
◎MISCELLANEOUS

S10 : FRONT SWITCH .... OPEN − CLOSE
S11 : INTER LOCK SWITCH .... OPEN − CLOSE
S12 : DISC DETECT SWITCH .... OPEN − CLOSE
S13 : HOME SWITCH .... OPEN − CLOSE

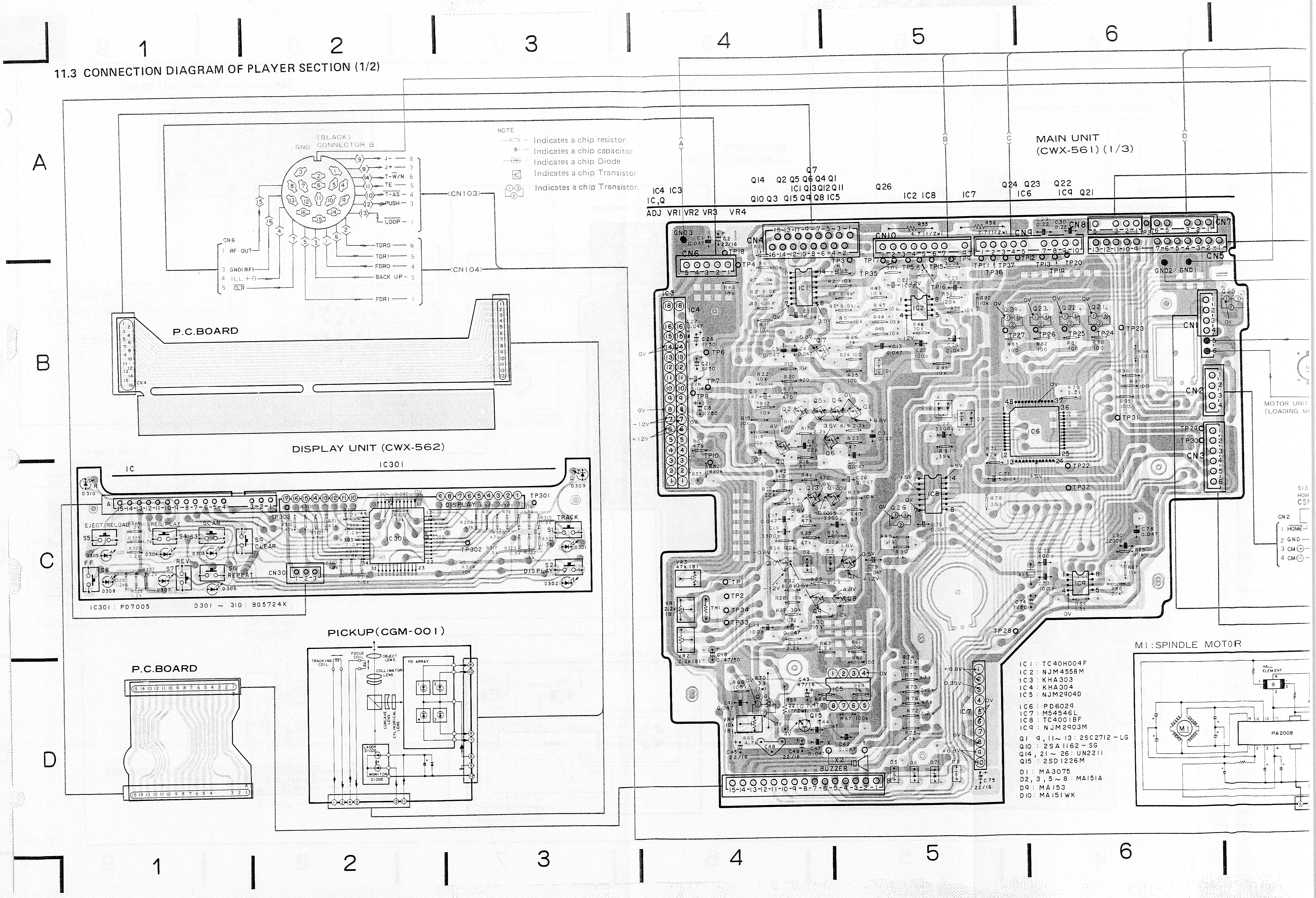
The underlined indicates the switch position.

Example of Display Operation

"a" segment is illuminated when:
Pa (pin 13) and G3 (pin 9) receives a signal.

"RPT" segment is illuminated when :
Ph (pin 16) and G3 (pin 9) receives a signal.

11.3 CONNECTION DIAGRAM OF PLAYER SECTION (1/2)


1
2
3
4
5
6
A
B
C
D
(BLACK)
CONNECTOR B
GND
J-
J+
T-W/N
TE
T-AS-
PUSH
LOOP
TDRO
TDRI
FDRO
BACK UP-
FDRI
CN103
CN104
CN6
RF-OUT
GND(RF)
ILL+B
CLR
P.C.BOARD
CN4
DISPLAY UNIT (CWX-562)
IC
IC301
EJECT/RELOAD
REV/PLAY
SCAN
CLEAR
TRACK
FF
REV
REPEAT
DISPLAY
CN301
TP301
TP302
TP303
IC301 : PD7005
D301 ~ 310 : BG5724K
PICKUP (CGM-001)
TRACKING COIL
FOCUS COIL
OBJECT LENS
COLLIMATOR LENS
CONCAVE LENS
CYLINDRICAL LENS
PD ARRAY
LASER DIODE
MONITOR DIODE
MAIN UNIT
(CWX-561) (1/3)
IC,Q
ADJ
VR1
VR2
VR3
VR4
IC4 IC3
Q14 Q2 Q5 Q6 Q4 Q1
Q7
IC1 Q13 Q12 Q11
Q10 Q3 Q15 Q9 Q8 IC5
Q26
IC2 IC8
IC7
Q24 Q23 Q22
IC6 IC9 Q21
GND3
GND2 GND1
CN2
CN3
CN5
CN7
CN8
CN9
CN10
BUZZER
X1
X2
MOTOR UNIT
(LOADING M
S13
HOM
CSI
HOME
GND
CM⊕
CM⊖
M1: SPINDLE MOTOR
HALL ELEMENT
PA2008

NOTE

- Indicates a chip resistor
- Indicates a chip capacitor
- Indicates a chip Diode
- Indicates a chip Transistor
- Indicates a chip Transistor.

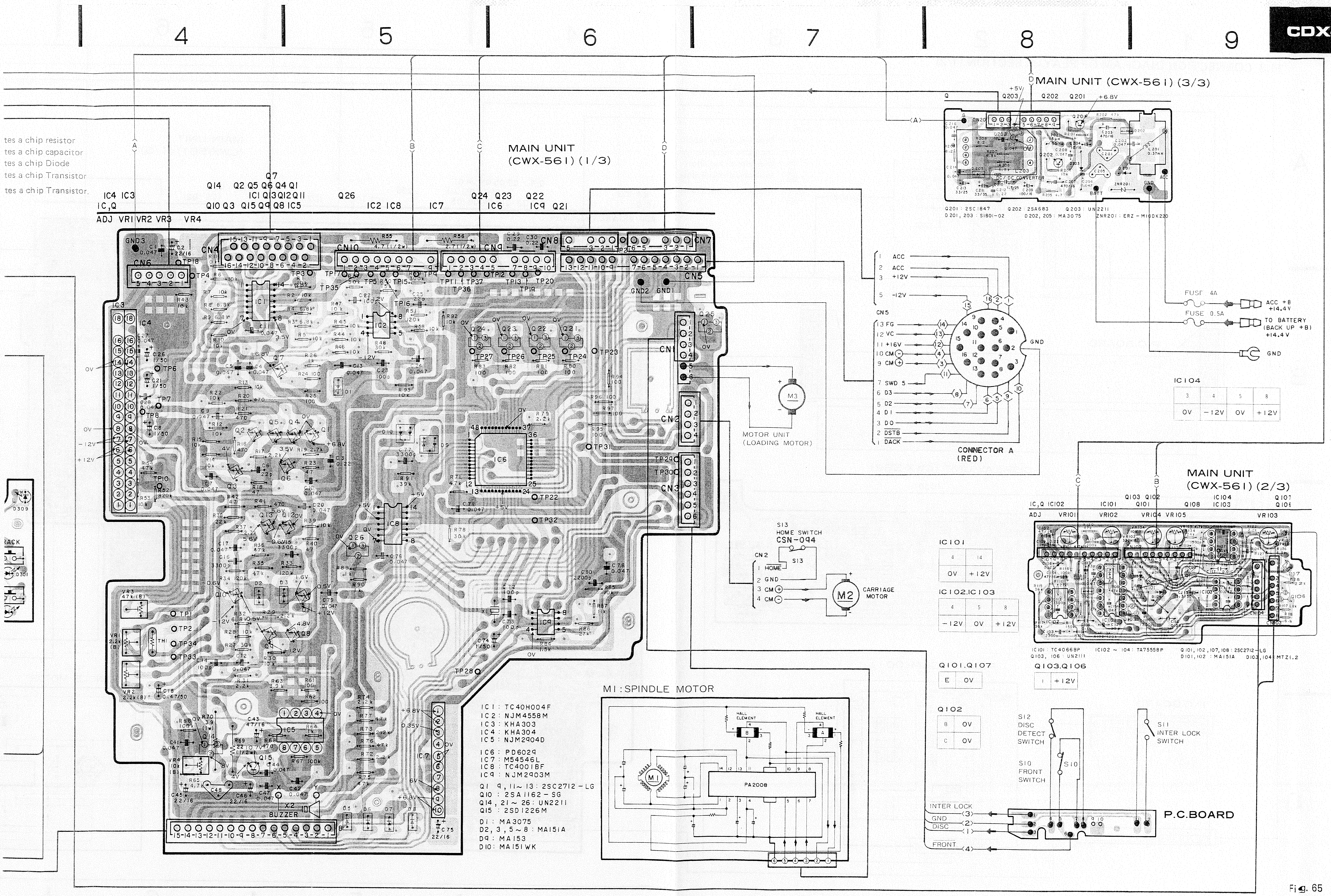
IC1 : TC40H004F
IC2 : NJM4558M
IC3 : KHA303
IC4 : KHA304
IC5 : NJM2904D

IC6 : PD6029
IC7 : M54546L
IC8 : TC4001BF
IC9 : NJM2903M

Q1 9, 11 ~ 13 : 2SC2712-LG
Q10 : 2SA1162-SG
Q14, 21 ~ 26 : UN2211
Q15 : 2SD1226M

D1 : MA3075
D2, 3, 5 ~ 8 : MA151A
D9 : MA153
D10 : MA151WK

tes a chip resistor
tes a chip capacitor
tes a chip Diode
tes a chip Transistor
tes a chip Transistor.


4
5
6
7
8
9
A
B
C
D
MAIN UNIT (CWX-561) (1/3)
MAIN UNIT (CWX-561) (3/3)
MAIN UNIT (CWX-561) (2/3)
IC,Q
ADJ
VR1 VR2 VR3 VR4
CN4
CN6
CN10
CN9
CN8
CN7
CN5
CN1
CN2
CN3
GND1
GND2
GND3
IC6
IC8
IC9
BUZZER
DC/DC CONVERTER
BATT
GND
ACC
FUSE 4A
FUSE 0.5A
ACC +B +14.4V
TO BATTERY (BACK UP +B) +14.4V
1 ACC
2 ACC
3 +12V
5 -12V
13 FG
12 VC
11 +16V
10 CM(−)
9 CM(+)
7 SWD 5
6 D3
5 D2
4 D1
3 D0
2 DSTB
1 DACK
CONNECTOR A (RED)
MOTOR UNIT (LOADING MOTOR)
M3
S13 HOME SWITCH CSN-094
1 HOME
2 GND
3 CM(+)
4 CM(−)
M2
CARRIAGE MOTOR
M1: SPINDLE MOTOR
HALL ELEMENT
PA2008
S12 DISC DETECT SWITCH
S10 FRONT SWITCH
S11 INTER LOCK SWITCH
INTER LOCK (3)
GND (2)
DISC (1)
FRONT (4)
P.C.BOARD
IC104: 3 0V, 4 −12V, 5 0V, 8 +12V
IC101: 4 0V, 14 +12V
IC102.IC103: 4 −12V, 5 0V, 8 +12V
Q101.Q107: E 0V
Q103.Q106: I +12V
Q102: B 0V, C 0V

IC1 : TC40H004F
IC2 : NJM4558M
IC3 : KHA303
IC4 : KHA304
IC5 : NJM2904D

IC6 : PD6029
IC7 : M54546L
IC8 : TC4001BF
IC9 : NJM2903M

Q1 9, 11～13 : 2SC2712－LG
Q10 : 2SA1162－SG
Q14, 21～26 : UN2211
Q15 : 2SD1226M

D1 : MA3075
D2, 3, 5～8 : MA151A
D9 : MA153
D10 : MA151WK

Q201 : 2SC1847　Q202 : 2SA683　Q203 : UN2211
D201, 203 : SIB01-02　D202, 205 : MA3075　ZNR201 : ERZ－M10DK220

IC101 : TC4066BP　IC102～104 : TA75558P　Q101, 102, 107, 108 : 2SC2712－LG
Q103, 106 : UN2111　D101, 102 : MA151A　D103, 104 : MTZ6.2

Fig. 65

- The Circuit diagram shown in Fig. 68 and 70 represent the circuits in the shaded area.
- Player Section

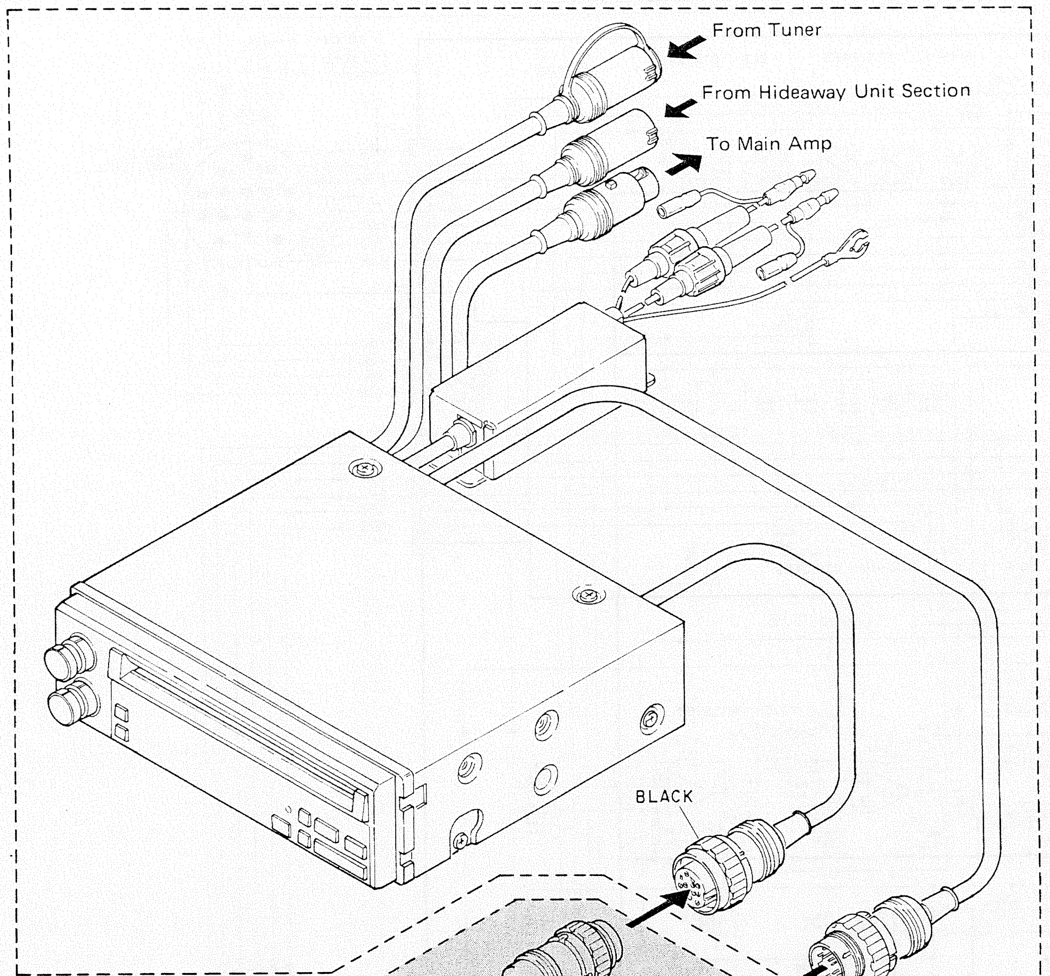

From Tuner
From Hideaway Unit Section
To Main Amp
BLACK
RED

Fig. 66

- Hideaway Unit Section

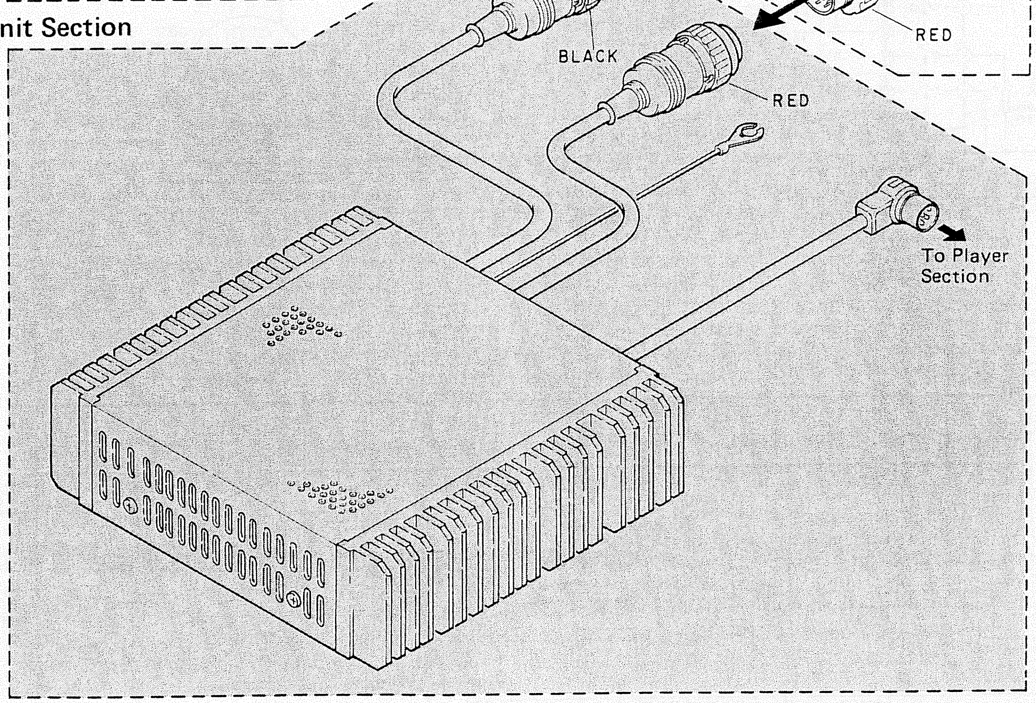
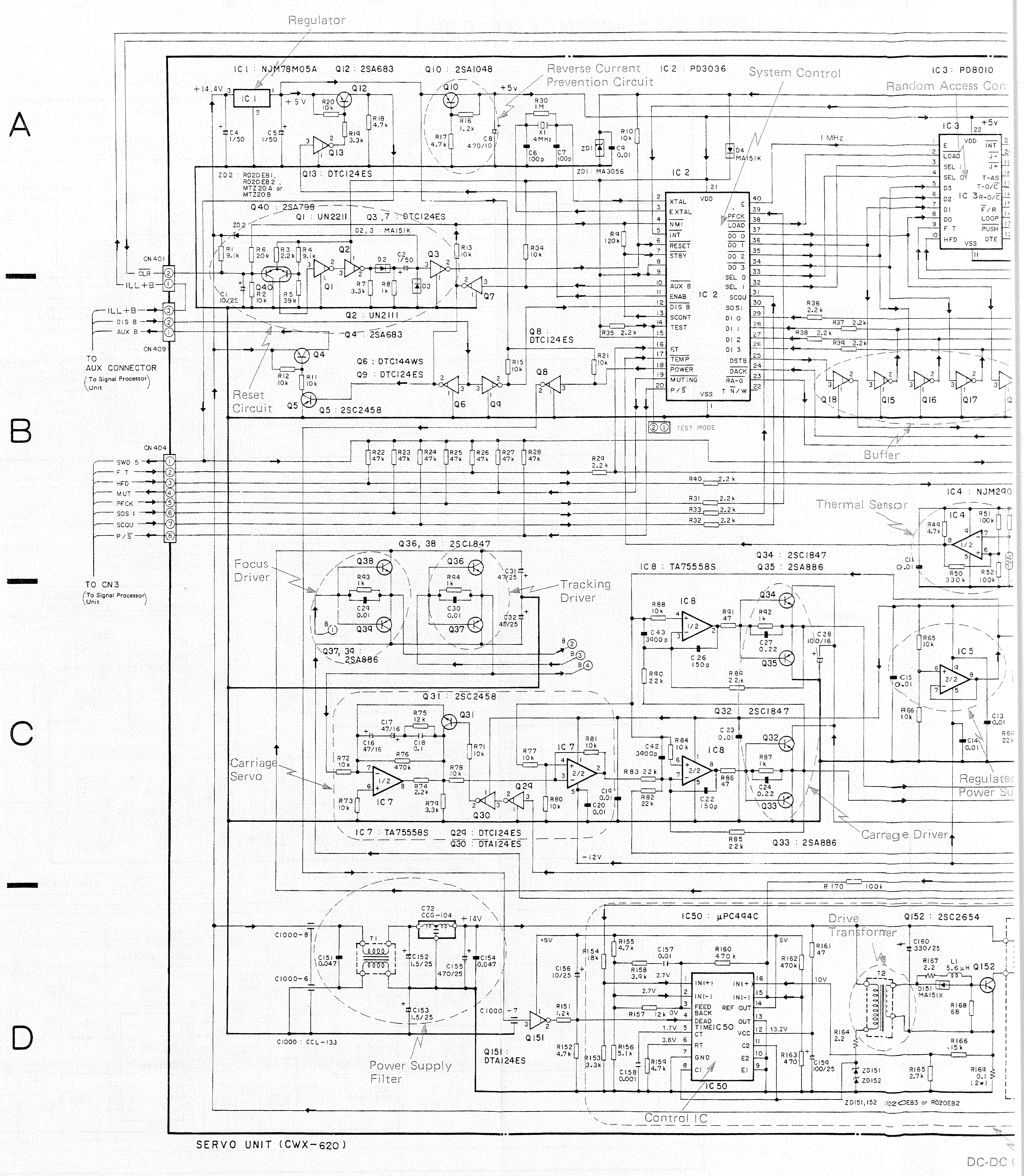

BLACK
RED
To Player Section

Fig. 67

11.4 SCHEMATIC DIAGRAM OF SERVO UNIT


1
2
3
A
B
C
D
Regulator
IC1 : NJM78M05A
Q12 : 2SA683
Q10 : 2SA1048
Reverse Current Prevention Circuit
IC2 : PD3036
System Control
IC3 : PD8010
Random Access Con
Q13 : DTC124ES
Q40 : 2SA798
Q1 : UN2211
Q3, 7 : DTC124ES
Q2 : UN2111
Q4 : 2SA683
Q6 : DTC144WS
Q9 : DTC124ES
Q5 : 2SC2458
Q8 DTC124ES
Reset Circuit
CN401
CLR
ILL+B
DIS B
AUX B
CN409
TO AUX CONNECTOR (To Signal Processor Unit)
CN404
SWO 5
F T
HFD
MUT
PFCK
SOS I
SCOU
P/S
TO CN3 (To Signal Processor Unit)
TEST MODE
Buffer
Thermal Sensor
IC4 : NJM290
Q36, 38 : 2SC1847
Q37, 39 : 2SA886
Focus Driver
Tracking Driver
IC8 : TA75558S
Q34 : 2SC1847
Q35 : 2SA886
IC5
Q31 : 2SC2458
Q32 : 2SC1847
Carriage Servo
IC7 : TA75558S
Q29 : DTC124ES
Q30 : DTA124ES
Q33 : 2SA886
Carrage Driver
Regulated Power Su
-12V
IC50 : µPC494C
Drive Transformer
Q152 : 2SC2654
Power Supply Filter
Q151 : DTA124ES
Control IC
C1000 : CCL-133
ZD151, 152 : RD2.0EB3 or RD20EB2
SERVO UNIT (CWX-620)
DC-DC

1 2 3 4 5 6

11.4 SCHEMATIC DIAGRAM OF SERVO UNIT

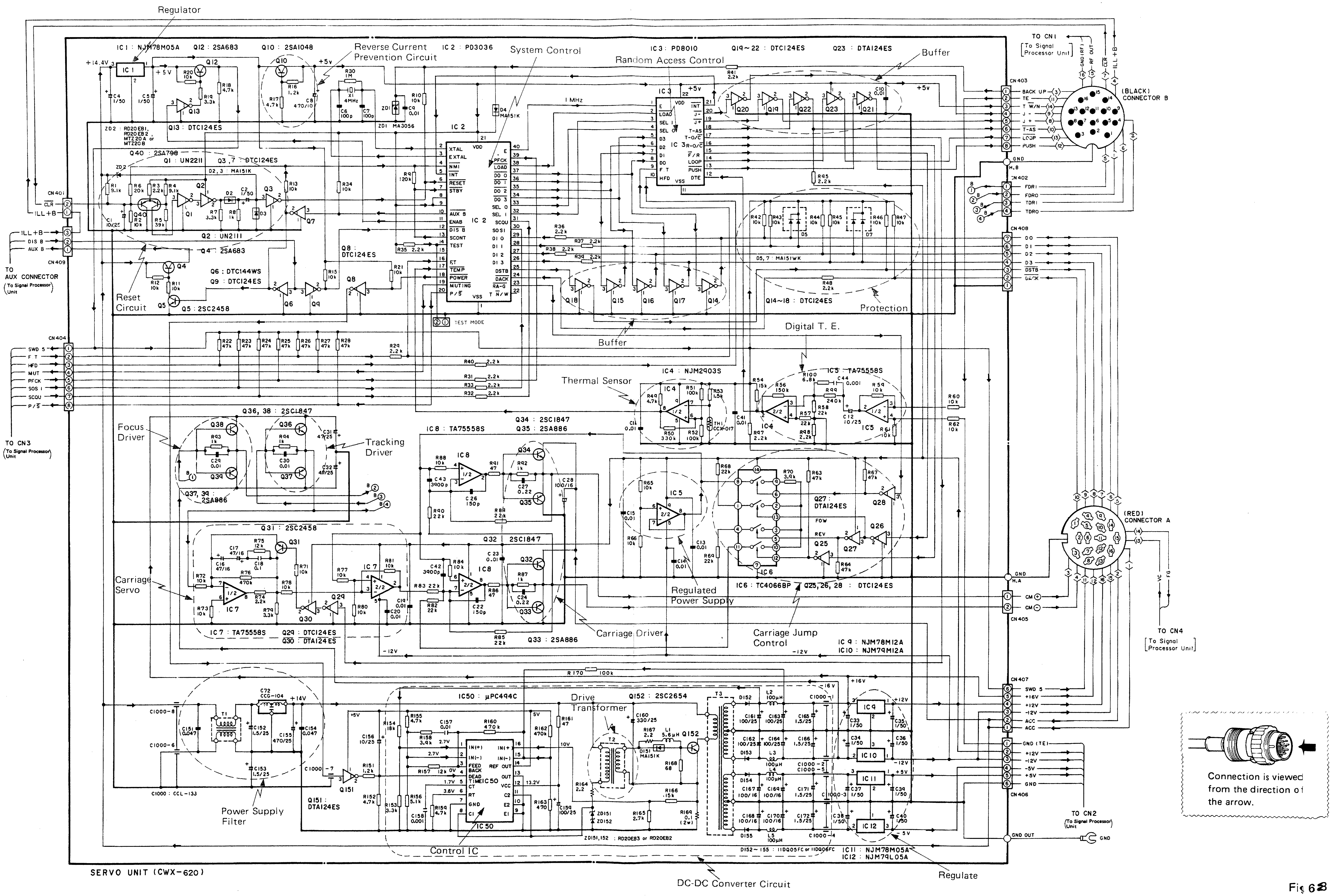
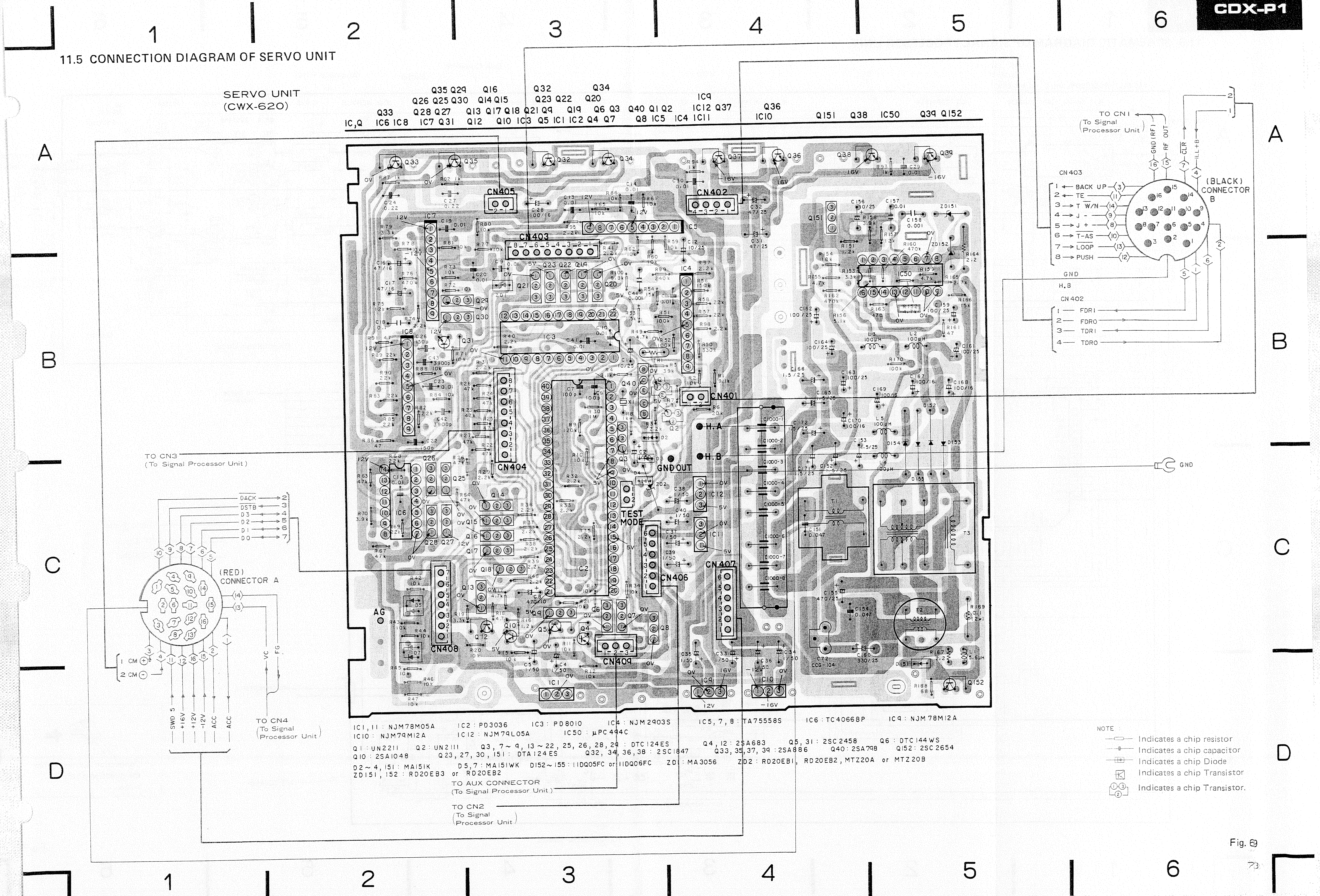

A
B
C
D
Regulator
IC1 : NJM78M05A
Q12 : 2SA683
Q10 : 2SA1048
Reverse Current Prevention Circuit
IC2 : PD3036
System Control
IC3 : PD8010
Random Access Control
Q19~22 : DTC124ES
Q23 : DTA124ES
Buffer
TO CN1 (To Signal Processor Unit)
(BLACK) CONNECTOR B
CN403
BACK UP
TE
T W/N
J+
J+
T-AS
LOOP
PUSH
GND
CN402
FDRI
FDRO
TDRI
TDRO
CN408
D0
D1
D2
D3
DSTB
DACK
ZD2 : RD20EB1, RD20EB2, MTZ20A or MTZ20B
Q13 : DTC124ES
Q40 : 2SA798
Q1 : UN2211
Q3, 7 : DTC124ES
D2, 3 : MA151K
Q2 : UN2111
Q4 : 2SA683
Q6 : DTC144WS
Q9 : DTC124ES
Q8 : DTC124ES
Q5 : 2SC2458
Reset Circuit
CN401
CLR
ILL+B
CN409
TO AUX CONNECTOR (To Signal Processor Unit)
TEST MODE
D5, 7 : MA151WK
Q14~18 : DTC124ES
Protection
Buffer
Digital T. E.
CN404
SWD 5
F T
HFD
MUT
PFCK
SOS 1
SCOU
P/S
TO CN3 (To Signal Processor Unit)
IC4 : NJM2903S
IC5 : TA75558S
Thermal Sensor
Q36, 38 : 2SC1847
Focus Driver
Tracking Driver
Q37, 39 : 2SA886
IC8 : TA75558S
Q34 : 2SC1847
Q35 : 2SA886
Q31 : 2SC2458
Q32 : 2SC1847
Carriage Servo
IC7 : TA75558S
Q29 : DTC124ES
Q30 : DTA124ES
Q33 : 2SA886
Carriage Driver
Regulated Power Supply
IC6 : TC4066BP
Q25, 26, 28 : DTC124ES
Q27 : DTA124ES
Carriage Jump Control
IC9 : NJM78M12A
IC10 : NJM79M12A
(RED) CONNECTOR A
GND H.A
CM+
CM−
CN405
TO CN4 (To Signal Processor Unit)
CN407
SWD 5
+16V
+12V
−12V
ACC
ACC
GND (TE)
+12V
−12V
−5V
+5V
GND
CN406
IC50 : μPC494C
Drive Transformer
Q152 : 2SC2654
Q151 : DTA124ES
Power Supply Filter
C1000 : CCL-133
Control IC
ZD151, 152 : RD20EB3 or RD20EB2
D152~155 : 11DQ05FC or 11DQ06FC
IC11 : NJM78M05A
IC12 : NJM79L05A
TO CN2 (To Signal Processor Unit)
GND OUT
Regulate
SERVO UNIT (CWX-620)
DC-DC Converter Circuit
Connection is viewed from the direction of the arrow.

Fig 63

1 2 3 4 5 6

11.5 CONNECTION DIAGRAM OF SERVO UNIT


1
2
3
4
5
6
A
B
C
D
SERVO UNIT
(CWX-620)
IC, Q
Q33 IC6 IC8
Q35 Q29 Q26 Q25 Q30 Q28 Q27 IC7 Q31
Q16 Q14 Q15 Q13 Q17 Q18 Q12
Q32 Q23 Q22 Q10 IC3 Q21 Q9 Q5 IC1
Q34 Q20 Q19 IC2 Q6 Q3 Q4 Q7
Q40 Q1 Q2 Q8 IC5
IC9 IC12 Q37 IC4 IC11
Q36 IC10
Q151 Q38 IC50 Q39 Q152
TO CN1
(To Signal Processor Unit)
GND (RF)
RF OUT
CLR
ILL+B
CN403
1 BACK UP
2 TE
3 T W/N
4 J -
5 J +
6 T-AS
7 LOOP
8 PUSH
(BLACK) CONNECTOR B
GND
H.B
CN402
1 FDR1
2 FDRO
3 TDR1
4 TDRO
GND
TO CN3
(To Signal Processor Unit)
DACK
DSTB
D3
D2
D1
D0
(RED) CONNECTOR A
1 CM
2 CM
SWD 5
+16V
+12V
-12V
ACC
ACC
VC
FG
TO CN4
(To Signal Processor Unit)
CN405
CN402
CN403
CN401
CN404
CN406
CN407
CN408
CN409
H.A
H.B
GND OUT
TEST MODE
AG
T1
T2
T3
IC50
1

IC1, 11 : NJM78M05A IC2 : PD3036 IC3 : PD8010 IC4 : NJM2903S IC5, 7, 8 : TA75558S IC6 : TC4066BP IC9 : NJM78M12A
IC10 : NJM79M12A IC12 : NJM79L05A IC50 : µPC494C

Q1 : UN2211 Q2 : UN2111 Q3, 7 ~ 9, 13 ~ 22, 25, 26, 28, 29 : DTC124ES Q4, 12 : 2SA683 Q5, 31 : 2SC2458 Q6 : DTC144WS
Q10 : 2SA1048 Q23, 27, 30, 151 : DTA124ES Q32, 34, 36, 38 : 2SC1847 Q33, 35, 37, 39 : 2SA886 Q40 : 2SA798 Q152 : 2SC2654

D2 ~ 4, 151 : MA151K D5, 7 : MA151WK D152 ~ 155 : 11DQ05FC or 11DQ06FC ZD1 : MA3056 ZD2 : RD20EB1, RD20EB2, MTZ20A or MTZ20B
ZD151, 152 : RD20EB3 or RD20EB2

TO AUX CONNECTOR
(To Signal Processor Unit)

TO CN2
(To Signal Processor Unit)

NOTE :

- Indicates a chip resistor
- Indicates a chip capacitor
- Indicates a chip Diode
- Indicates a chip Transistor
- Indicates a chip Transistor.

Fig. 69

11.6 SCHEMATIC DIAGRAM OF SIGNAL PROCESSOR UNIT

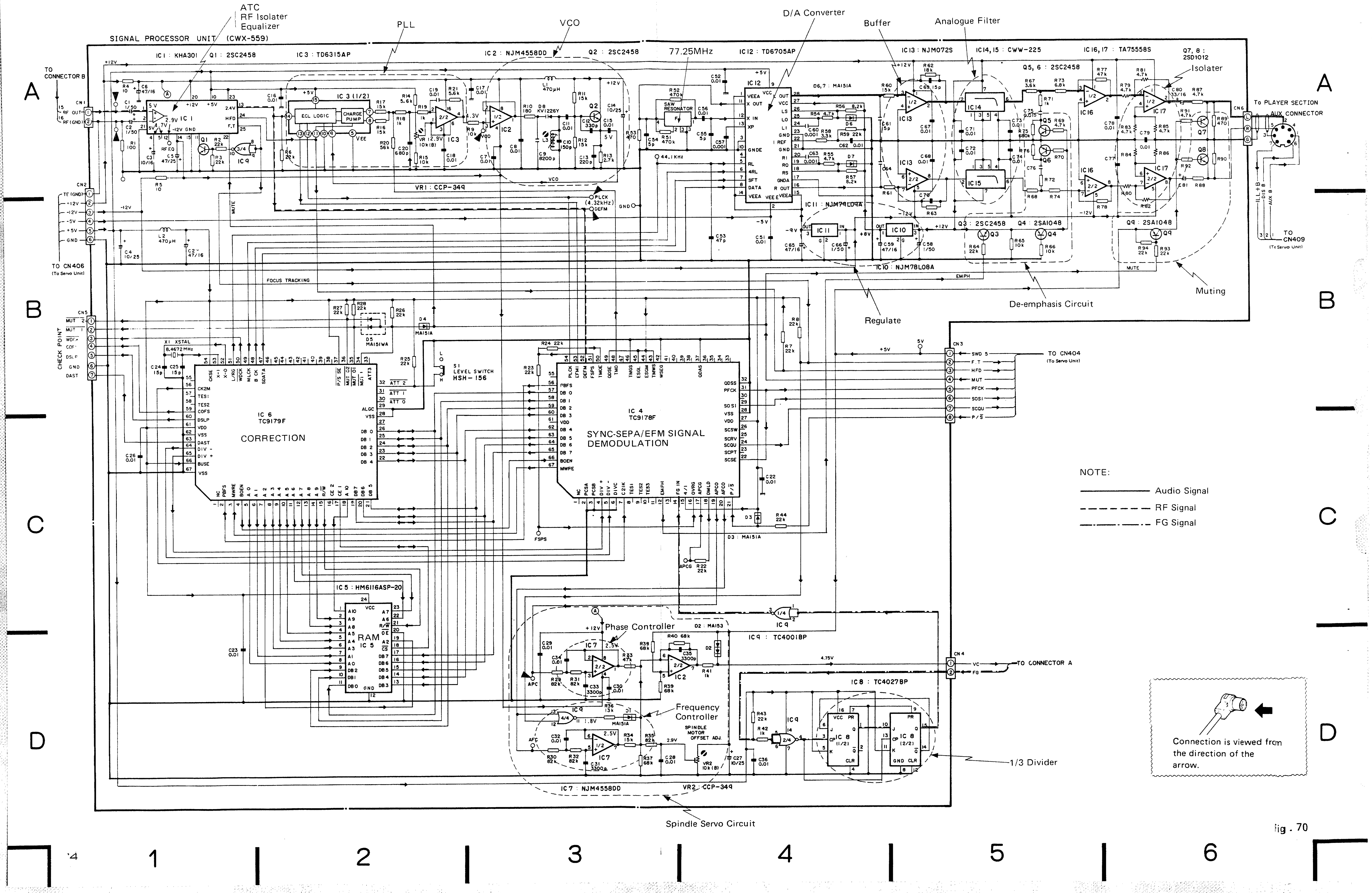
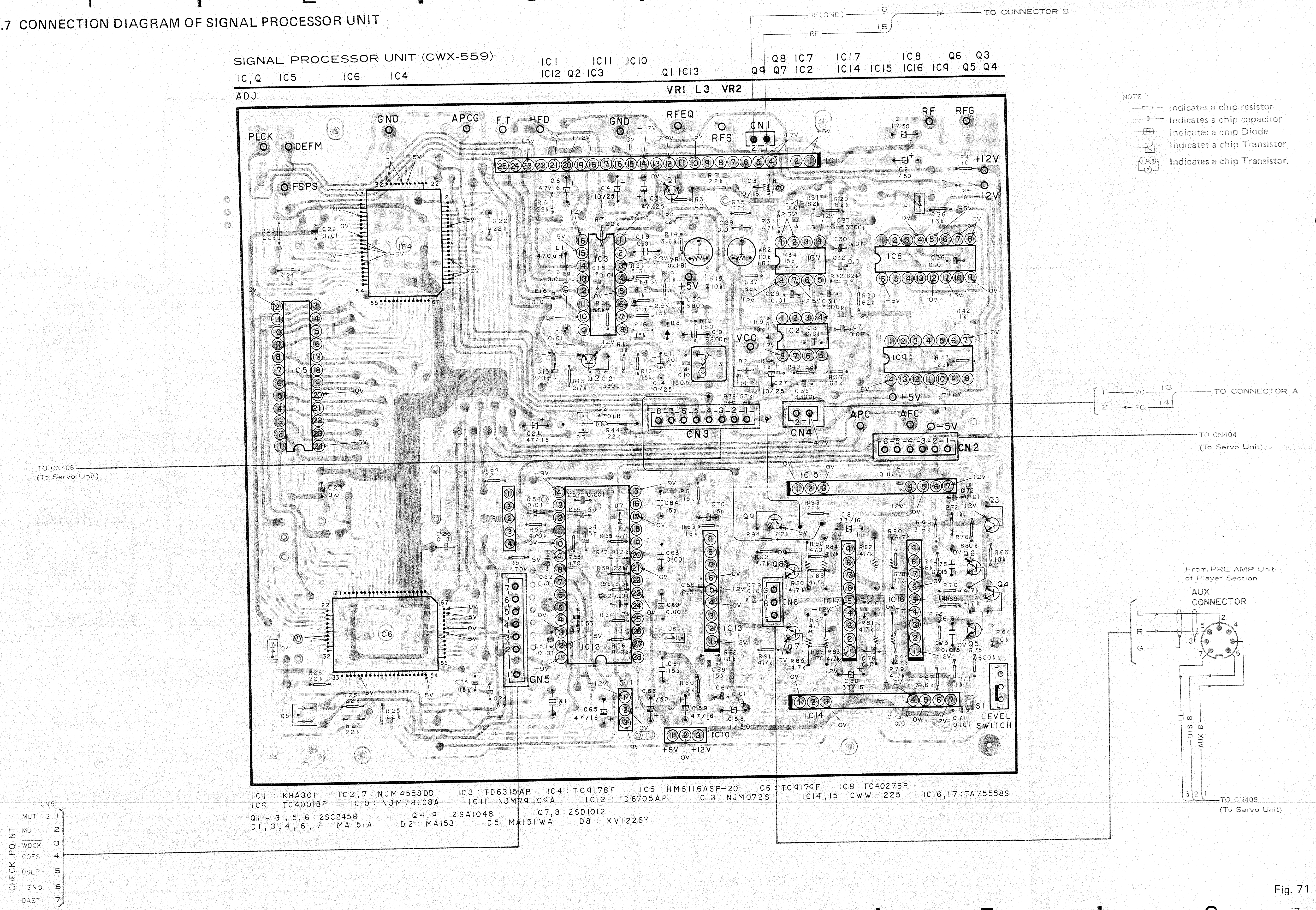

SIGNAL PROCESSOR UNIT (CWX-559)
ATC
RF Isolater
Equalizer
PLL
VCO
D/A Converter
Buffer
Analogue Filter
Isolater
IC1 : KHA301
Q1 : 2SC2458
IC3 : TD6315AP
IC2 : NJM4558DD
Q2 : 2SC2458
77.25MHz
IC12 : TD6705AP
IC13 : NJM072S
IC14, 15 : CWW-225
IC16, 17 : TA75558S
Q7, 8 : 2SD1012
Q5, 6 : 2SC2458
D6, 7 : MA151A
IC11 : NJM79L04A
IC10 : NJM78L08A
Q3 : 2SC2458
Q4 : 2SA1048
Q9 : 2SA1048
Regulate
De-emphasis Circuit
Muting
TO CONNECTOR B
CN1
RF OUT
RF (GND)
CN2
TE (GND)
+12V
-12V
-5V
+5V
GND
TO CN406 (To Servo Unit)
CN5
CHECK POINT
MUT 2
MUT 1
WDCK
COFS
DSLP
GND
DAST
VR1 : CCP-349
PLCK (4.32kHz)
DEFM
44.1kHz
FOCUS TRACKING
MUTE
EMPH
SAW RESONATOR
CN6
To PLAYER SECTION
AUX CONNECTOR
TO CN409 (To Servo Unit)
X1 XSTAL 8.4672MHz
D5 MA151WA
D4 MA151A
S1 LEVEL SWITCH HSH-156
ATT 2
ATT 1
ATT 0
IC6 TC9179F
CORRECTION
IC4 TC9178F
SYNC-SEPA/EFM SIGNAL DEMODULATION
CN3
TO CN404 (To Servo Unit)
SWD 5
F.T
HFD
MUT
PFCK
SOSI
SCQU
P/S
FSPS
D3 : MA151A
APCG
IC5 : HM6116ASP-20
RAM IC5
Phase Controller
IC7
D2 : MA153
IC9 : TC4001BP
CN4
TO CONNECTOR A
4.75V
VC
FG
APC
AFC
Frequency Controller
SPINDLE MOTOR OFFSET ADJ.
VR2 10k (B)
IC8 : TC4027BP
1/3 Divider
IC7 : NJM4558DD
VR2 : CCP-349
Spindle Servo Circuit
NOTE:
Audio Signal
RF Signal
FG Signal
Connection is viewed from the direction of the arrow.
1
2
3
4
5
6
A
B
C
D

Fig. 70

11.7 CONNECTION DIAGRAM OF SIGNAL PROCESSOR UNIT

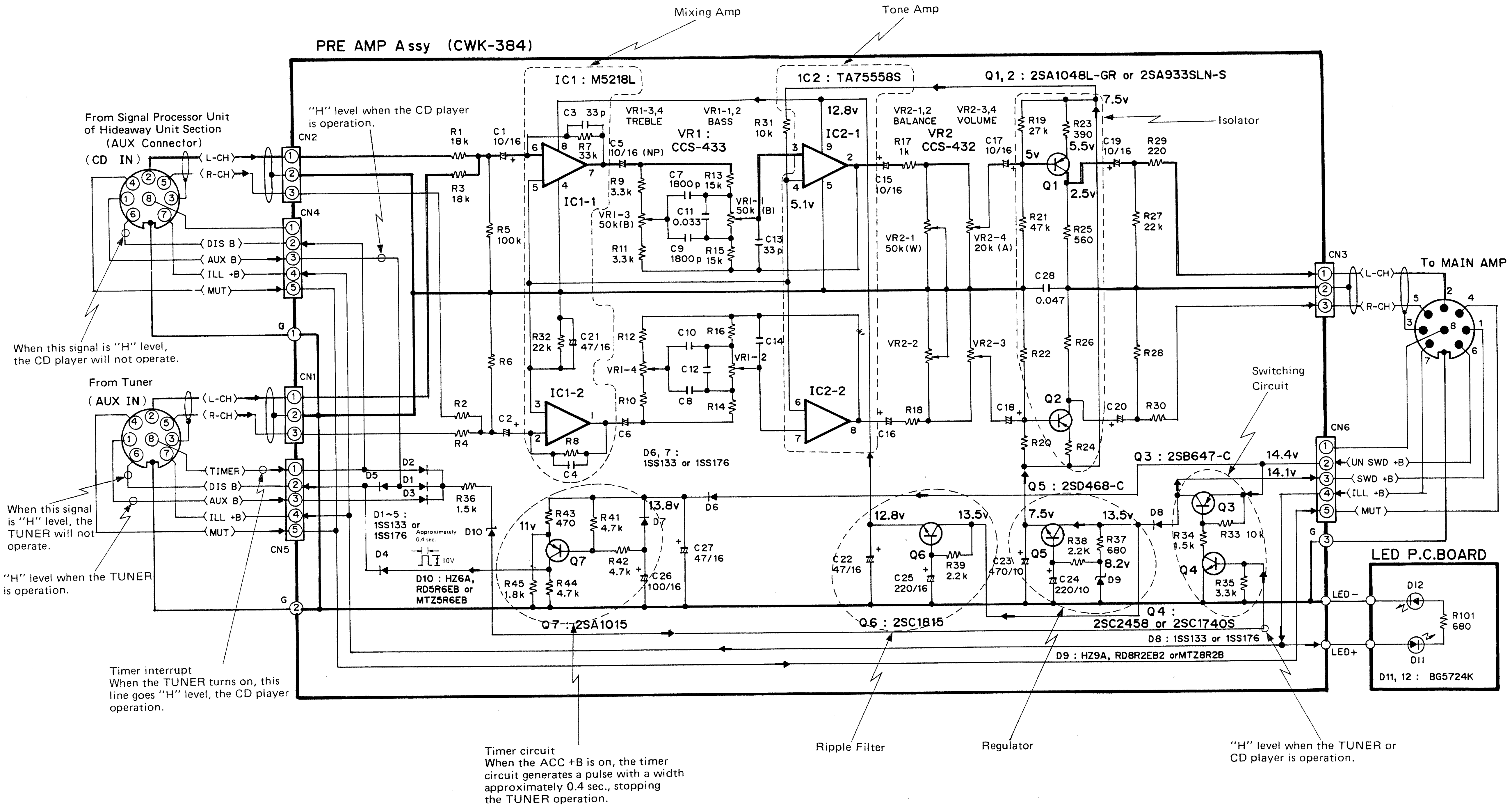

SIGNAL PROCESSOR UNIT (CWX-559)
IC, Q ADJ
IC5 IC6 IC4
IC1 IC12 Q2 IC11 IC3 IC10
Q1 IC13 VR1 L3 VR2
Q9 Q8 Q7 IC7 IC2 IC17 IC14 IC15 IC8 IC16 IC9 Q6 Q5 Q3 Q4
RF(GND) 16
RF 15
TO CONNECTOR B
PLCK
DEFM
FSPS
GND
APCG
F.T
HFD
RFEQ
RFS
CN1
RF
RFG
+12V
-12V
VCO
+5V
APC
AFC
-5V
CN3
CN4
CN2
CN5
CN6
X1
1 VC 13
2 FG 14
TO CONNECTOR A
TO CN404 (To Servo Unit)
TO CN406 (To Servo Unit)
S1 LEVEL SWITCH
From PRE AMP Unit of Player Section
AUX CONNECTOR
L
R
G
ILL
DIS B
AUX B
TO CN409 (To Servo Unit)
CHECK POINT
CN5
MUT 2 1
MUT 1 2
WDCK 3
COFS 4
DSLP 5
GND 6
DAST 7

NOTE :
Indicates a chip resistor
Indicates a chip capacitor
Indicates a chip Diode
Indicates a chip Transistor
Indicates a chip Transistor.

IC1 : KHA301 IC2,7 : NJM4558DD IC3 : TD6315AP IC4 : TC9178F IC5 : HM6116ASP-20 IC6 : TC9179F IC8 : TC4027BP
IC9 : TC4001BP IC10 : NJM78L08A IC11 : NJM79L09A IC12 : TD6705AP IC13 : NJM072S IC14,15 : CWW-225 IC16,17 : TA75558S
Q1 ~ 3, 5, 6 : 2SC2458 Q4,9 : 2SA1048 Q7,8 : 2SD1012
D1, 3, 4, 6, 7 : MA151A D2 : MA153 D5 : MA151WA D8 : KV1226Y

Fig. 71

11.8 SCHEMATIC DIAGRAM OF PLAYER SECTION (2/2)


Mixing Amp
Tone Amp
PRE AMP Assy (CWK-384)
IC1 : M5218L
IC2 : TA75558S
Q1, 2 : 2SA1048L-GR or 2SA933SLN-S
Isolator
From Signal Processor Unit of Hideaway Unit Section (AUX Connector)
(CD IN)
"H" level when the CD player is operation.
L-CH
R-CH
DIS B
AUX B
ILL +B
MUT
CN2
CN4
CN1
CN5
CN3
CN6
G
When this signal is "H" level, the CD player will not operate.
From Tuner
(AUX IN)
TIMER
When this signal is "H" level, the TUNER will not operate.
"H" level when the TUNER is operation.
R1 18k
R2
R3 18k
R4
R5 100k
R6
C1 10/16
C2
C3 33p
R7 33k
C4
C5 10/16 (NP)
C6
VR1-3,4 TREBLE
VR1-1,2 BASS
VR1 : CCS-433
R9 3.3k
R11 3.3k
C7 1800p
C9 1800p
C11 0.033
R13 15k
R15 15k
VR1-1 50k(B)
VR1-3 50k(B)
C13 33p
R31 10k
12.8v
IC2-1
5.1v
IC1-1
IC1-2
IC2-2
R8
R32 22k
C21 47/16
R12
C10
R16
C14
VR1-4
C12
VR1-2
R10
C8
R14
VR2-1,2 BALANCE
VR2-3,4 VOLUME
VR2 CCS-432
R17 1k
C15 10/16
C17 10/16
VR2-1 50k(W)
VR2-4 20k(A)
VR2-2
VR2-3
R18
C16
C18
R19 27k
R23 390
5v
5.5v
7.5v
Q1
2.5v
C19 10/16
R29 220
R21 47k
R25 560
R27 22k
C28 0.047
R22
R26
R28
Q2
C20
R30
R20
R24
To MAIN AMP
Switching Circuit
Q3 : 2SB647-C
14.4v
14.1v
UN SWD +B
SWD +B
D2
D5
D1
D3
R36 1.5k
D1~5 : 1SS133 or 1SS176
Approximately 0.4 sec.
10V
D10
D4
D10 : HZ6A, RD5R6EB or MTZ5R6EB
R43 470
R41 4.7k
11v
Q7
R42 4.7k
R45 1.8k
R44 4.7k
13.8v
D7
D6
C26 100/16
C27 47/16
D6, 7 : 1SS133 or 1SS176
Q7 : 2SA1015
12.8v
13.5v
Q6
C22 47/16
C25 220/16
R39 2.2k
Q6 : 2SC1815
Q5 : 2SD468-C
7.5v
13.5v
Q5
R38 2.2K
R37 680
8.2v
C23 470/10
C24 220/10
D9
D8
Q3
R34 1.5k
R33 10k
Q4
R35 3.3k
Q4 : 2SC2458 or 2SC1740S
D8 : 1SS133 or 1SS176
D9 : HZ9A, RD8R2EB2 or MTZ8R2B
LED P.C.BOARD
LED−
LED+
D12
D11
R101 680
D11, 12 : BG5724K

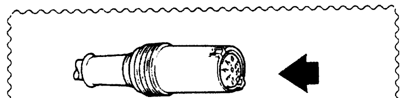
Timer interrupt
When the TUNER turns on, this line goes "H" level, the CD player operation.

Timer circuit
When the ACC +B is on, the timer circuit generates a pulse with a width approximately 0.4 sec., stopping the TUNER operation.

Ripple Filter

Regulator

"H" level when the TUNER or CD player is operation.

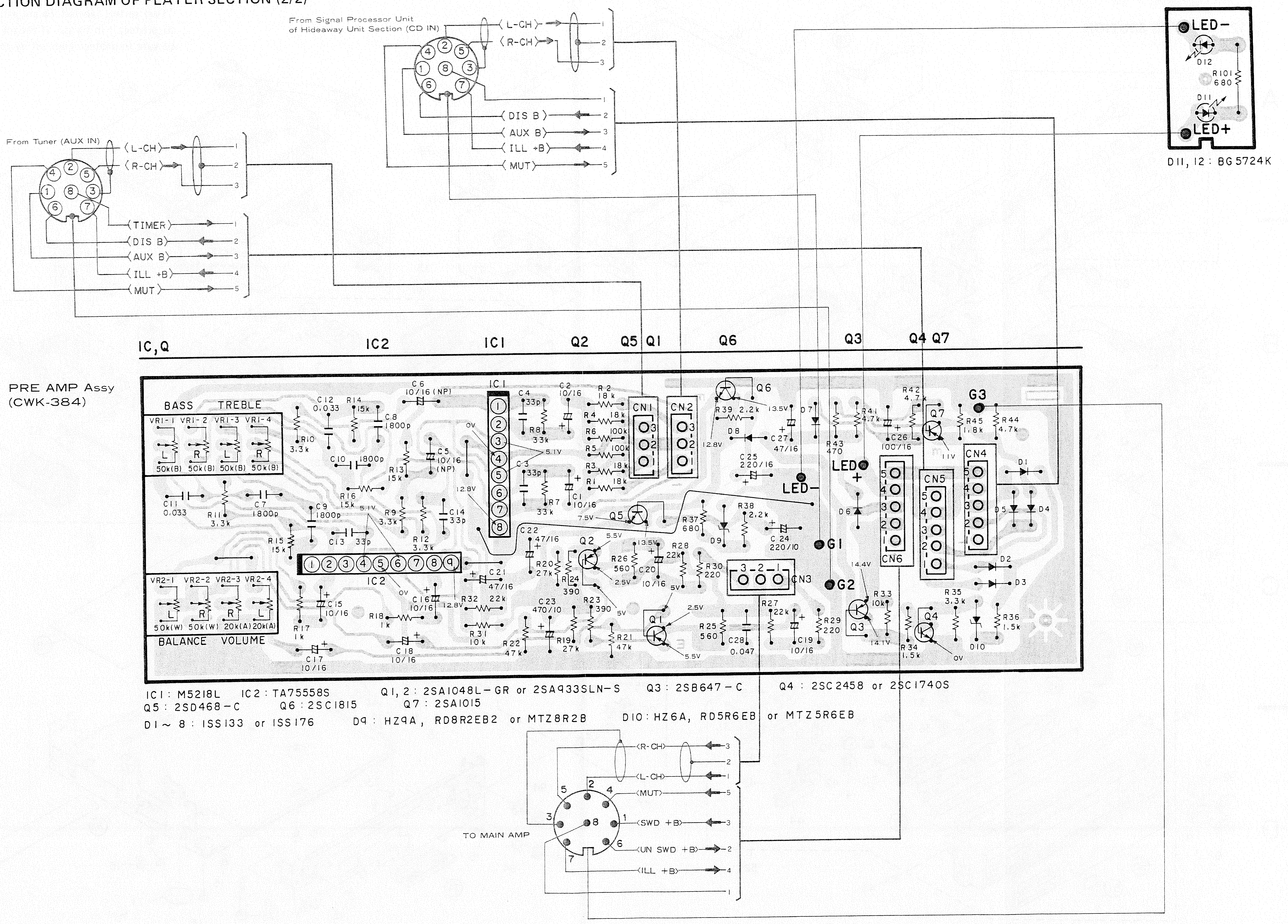


Connection is viewed from the direction of the arrow.

NOTE:
When the TUNER is connected, the priority of operation is as follows:
1. When the TUNER timer turns on while the CD player is in operation, the unit enters the tuner mode.
2. When a disc is loaded into the CD player while the TUNER is in operation, the TUNER stops operation and the CD player starts operation.

Fig. 72

11.9 CONNECTION DIAGRAM OF PLAYER SECTION (2/2)


LED P.C. BOARD
LED−
LED+
D12
D11
R101 680
D11, 12 : BG5724K
From Signal Processor Unit of Hideaway Unit Section (CD IN)
From Tuner (AUX IN)
L-CH
R-CH
TIMER
DIS B
AUX B
ILL +B
MUT
PRE AMP Assy (CWK-384)
IC, Q
IC2
IC1
Q2
Q5 Q1
Q6
Q3
Q4 Q7
BASS
TREBLE
VR1-1
VR1-2
VR1-3
VR1-4
VR2-1
VR2-2
VR2-3
VR2-4
BALANCE
VOLUME
CN1
CN2
CN3
CN4
CN5
CN6
G1
G2
G3
LED+
LED−
TO MAIN AMP
R-CH
L-CH
MUT
SWD +B
UN SWD +B
ILL +B

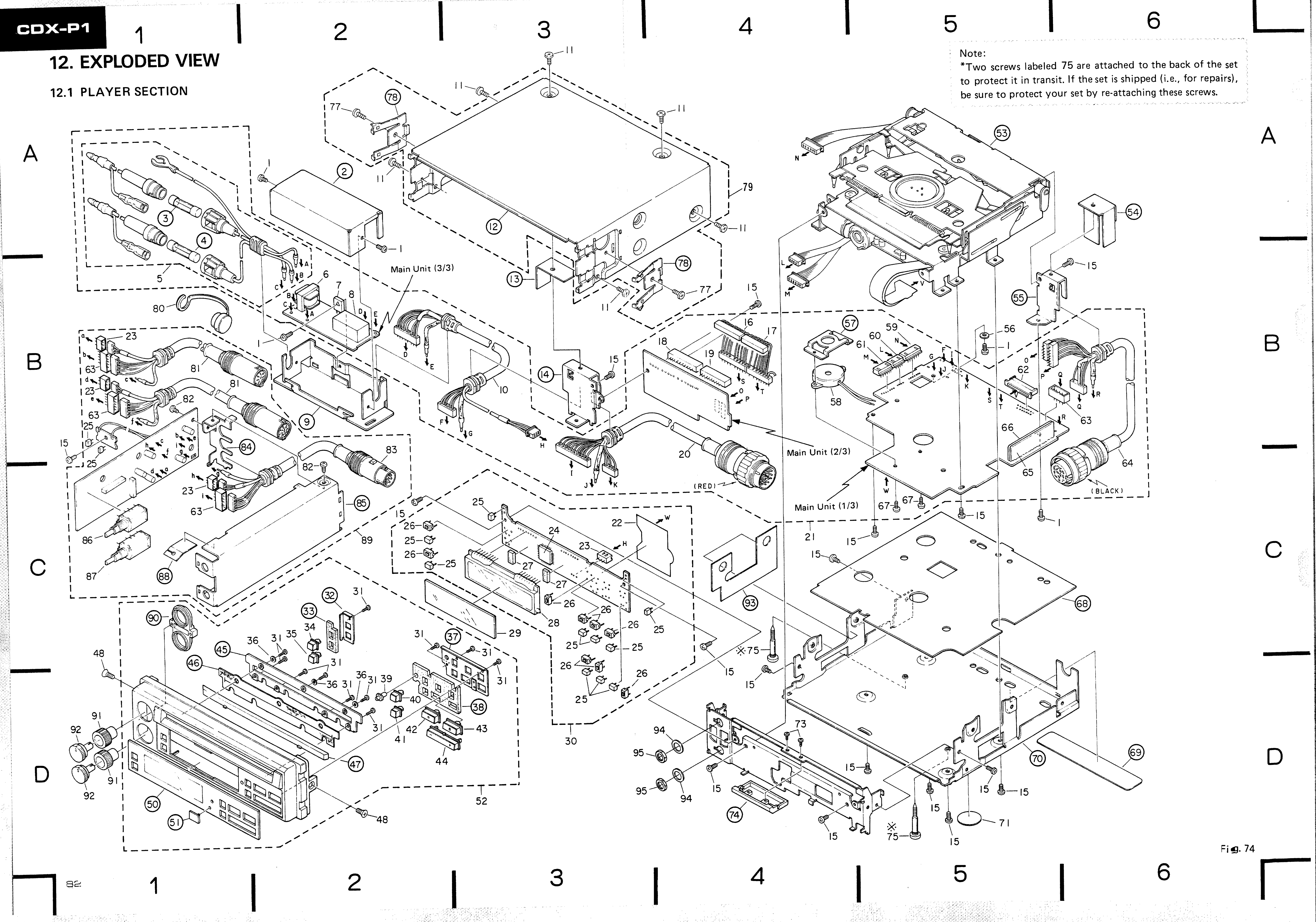
IC1 : M5218L IC2 : TA75558S Q1, 2 : 2SA1048L−GR or 2SA933SLN−S Q3 : 2SB647−C Q4 : 2SC2458 or 2SC1740S
Q5 : 2SD468−C Q6 : 2SC1815 Q7 : 2SA1015
D1 ~ 8 : 1SS133 or 1SS176 D9 : HZ9A, RD8R2EB2 or MTZ8R2B D10 : HZ6A, RD5R6EB or MTZ5R6EB

Fig. 73

12. EXPLODED VIEW

12.1 PLAYER SECTION

Note:
*Two screws labeled 75 are attached to the back of the set to protect it in transit. If the set is shipped (i.e., for repairs), be sure to protect your set by re-attaching these screws.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A
B
C
D
Main Unit (3/3)
Main Unit (2/3)
Main Unit (1/3)
(RED)
(BLACK)
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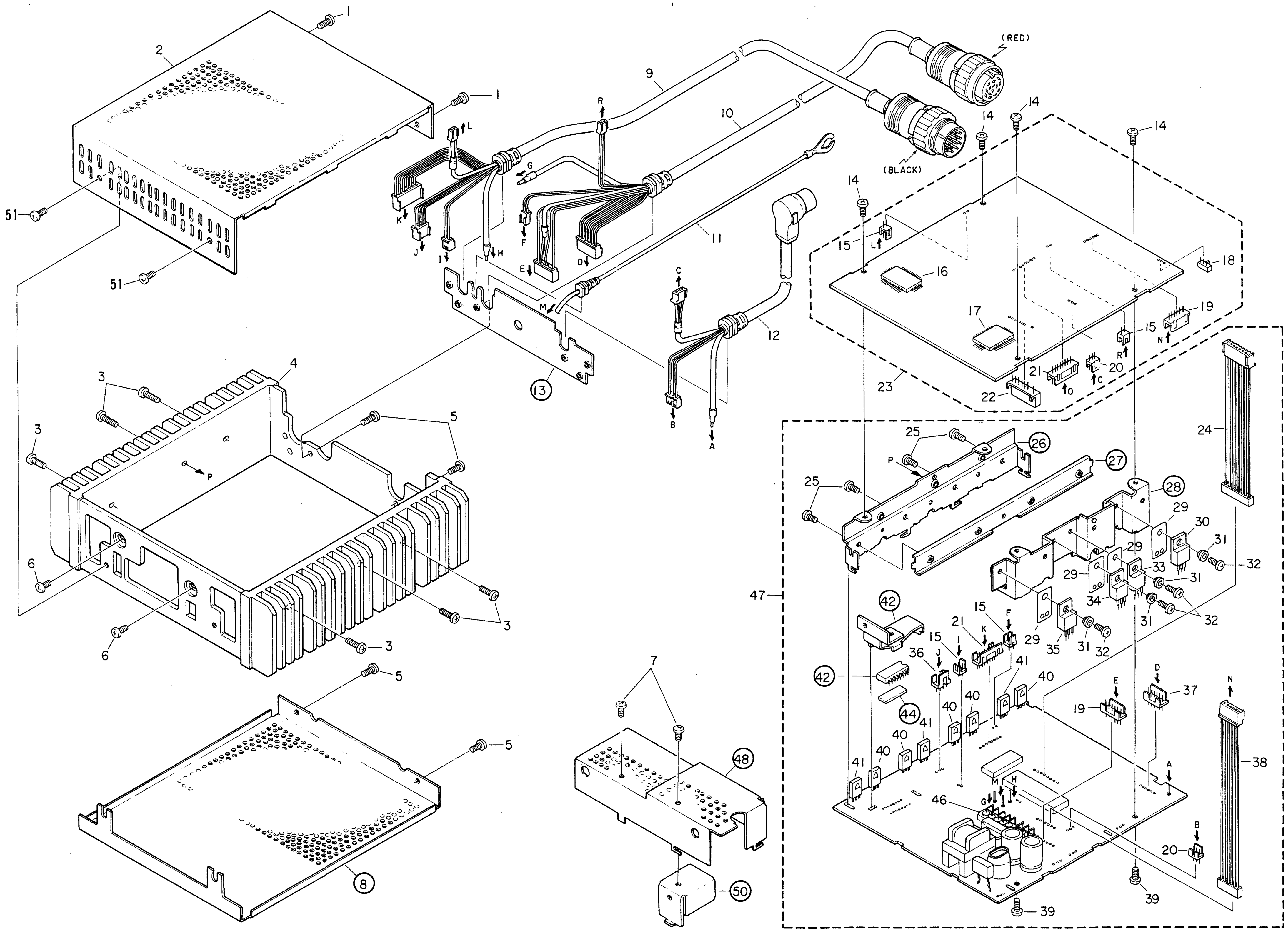
Fig. 74

- **Hideaway Unit Section**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(BLACK)
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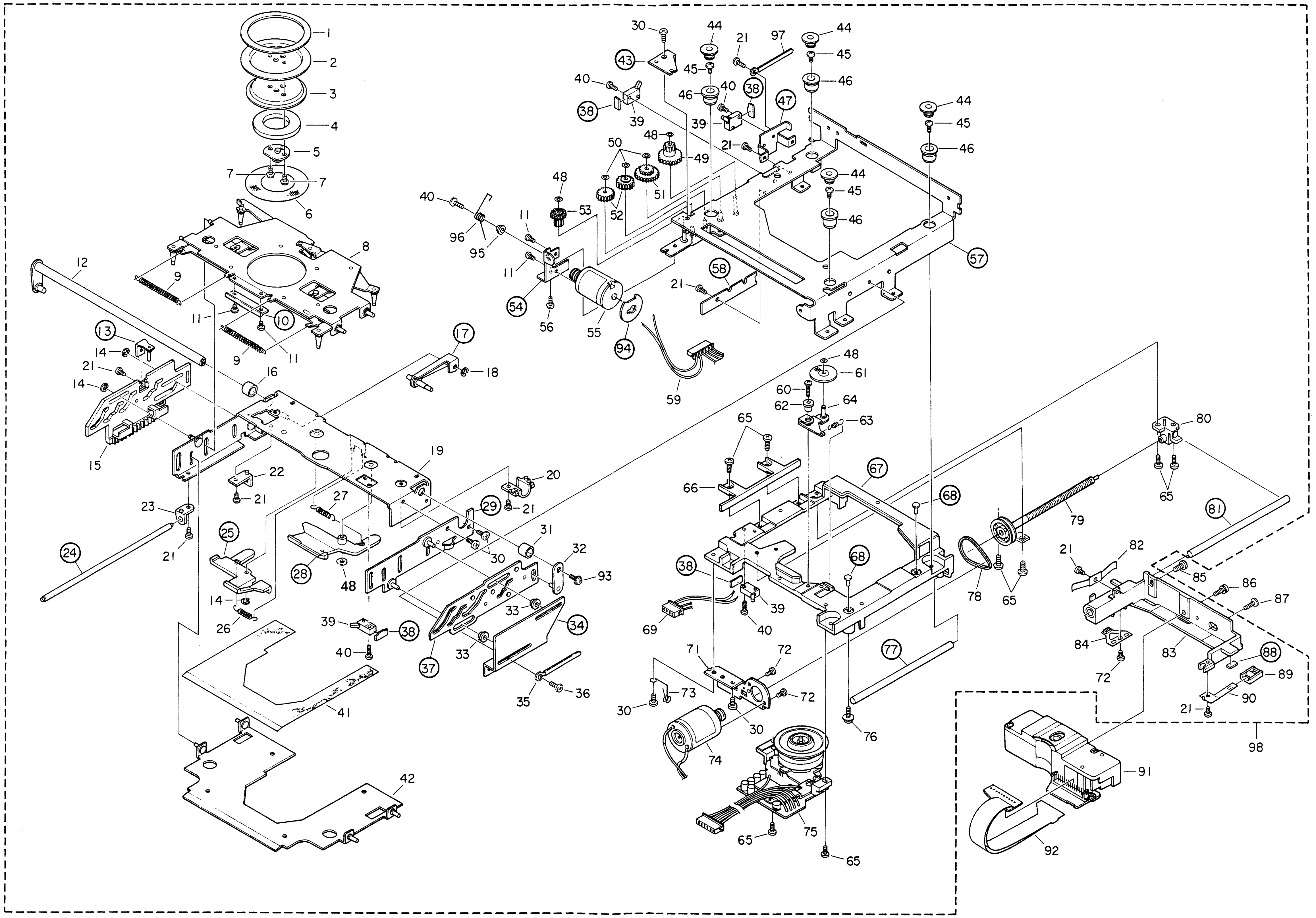
Fig. 75

12.3 MECHANISM ASSY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Fg. 76

• Parts List

NOTE

- *For your Parts Stock Control, the fast moving items are indicated with the marks ★★ and ★.*
  ★★ : GENERALLY MOVES FASTER THAN ★.
  This classification shall be adjusted by each distributor because it depends on model number, temperature, humidity, etc.
- *Parts whose parts numbers are omitted are subject to being not supplied.*

Mark	No.	Part No.	Description
	1.	BMZ26P050FMC	Screw
	2.		Cover
	3.		Fuse, 0.5A
	4.		Fuse, 4A
	5.	CDF-896	Cord
	6.	CTF-235	Coil, 0.37mH
★★	7.	2SC1847	Transistor
	8.	CTX-073	Transformer
	9.		Holder
	10.	CDF-895	Cord
	11.	CBA-121	Screw, M3 x 4 (CDX-P1/ES, EW)
		CBA-184	Screw, M3 x 4 (CDX-P1/US)
	12.		Case
	13.		Insulator
	14.		Holder
	15.	BMZ26P040FMC	Screw
	16.	CDF-892	Connector (9P)
	17.	CDF-891	Connector (8P)
	18.	CKS-574	Plug (9P)
	19.	CKS-573	Plug (8P)
	20.	CDF-893	Connector
	21.	CWX-561	Main Unit
	22.	CNL-773	P.C. Board
	23.	CKS-567	Plug (3P)
★★	24.	PD7005	IC
★	25.	BG5724K	LED
★★	26.	CSG-212	Switch
	27.	CNN-207	Spacer
	28.	CP2131GLR	Display
	29.	CNN-369	Film
	30.	CWX-562	Display Unit
	31.	PVZ14P045FZK	Screw
	32.		Holder
	33.		Cushion
★	34.	CAC-849	Button (TRACK) (CDX-P1/ES, EW)
		CAE-079	Button (TRACK) (CDX-P1/US)
★	35.	CAC-852	Button (DISPLAY) (CDX-P1/ES, EW)
		CAE-082	Button (DISPLAY) (CDX-P1/US)
	36.	HBF-193	Washer
	37.		Holder
	38.		Cushion
★	39.	CAA-605	Button (CLER)
★	40.	CAC-850	Button (SCAN) (CDX-P1/ES, EW)
		CAE-080	Button (SCAN) (CDX-P1/US)

Mark	No.	Part No.	Description
★	41.	CAC-851	Button (REPEAT) (CDX-P1/ES, EW)
		CAE-081	Button (REPEAT) (CDX-P1/US)
★	42.	CAE-003	Button (REL/PLAY) (CDX-P1/ES, EW)
		CAE-084	Button (REL/PLAY) (CDX-P1/ES, EW)
★	43.	CAC-847	Button (EJECT/RELOAD)
★	44.	CAC-853	Button (FF, REV) (DCX-P1/ES, EW)
		CAE-083	Button (FF, REV) (CDX-P1/US)
	45.		Holder
	46.		Cover
	47.		Lens
	48.	CMZ30P050FMC	Screw
	49.		Grille
	50.		Plate
	51.		Badge
	52.	CXD-688	Grille Assy (CDX-P1/ES, EW)
		CXD-690	Grille Assy (CDX-P1/US)
	53.		Mechanism Assy
	54.		Insulator
	55.		Holder
	56.	WA26W060C50	Washer
	57.		Holder
	58.	CPV-031	Buzzer
	59.	CKS-554	Plug (6P)
	60.	CKS-470	Plug (4P)
	61.	CKS-472	Plug (6P)
	62.	CKS-417	Connector (16P)
	63.	CKS-569	Plug (5P)
	64.	CDF-894	Connector
★★	65.	KHA303	IC
★★	66.	KHA304	IC
	67.	BMZ20P050FMC	Screw
	68.		Insulator
	69.		Seal
	70.		Chassis
	71.	CNM-153	Seal
	72.		Frame
	73.	CBA-126	Screw, M2 x 4
	74.		Guide
	75.	CBA-154	Screw
	76.	VACANT	
	77.	BMZ30P030FZK	Screw
	78.		Spring
	79.	CXD-692	Case Unit (CDX-P1/ES, EW)
		CXD-693	Case Unit (CDX-P1/US)
	80.	CNW-765	Cap

Mark	No.	Part No.	Description
	81.	CDK-256	Cord
	82.	PMS26P040FUC	Screw
	83.	CDK-257	Cord
	84.		Bracket
	85.		Shield
★★	86.	CCS-432	Volume (BALANCE/VOLUME)
★★	87.	CCS-433	Volume (BASS/TREBLE)
	88.		Holder
	89.	CWK-384	Pre Amp Assy
	90.		Cover
★	91.	CAA-651	Knob (BALANCE, BASS) (CDX-P1/ES, EW)
		CAA-653	Knob (BALANCE, BASS) (CDX-P1/US)
★	92.	CAA-650	Knob (VOLUME, TREBLE) (CDX-P1/ES, EW)
		CAA-652	Knob (VOLUME, TREBLE) (CDX-P1/US)
	93.		Insulator
	94.	CBE-086	Washer (M7)
	95.	CBN-032	Nut (M7)

12.2 HIDEAWAY UNIT SECTION

NOTE:

- *For your parts Stock Control, the fast moving items are indicated with the marks ★★ and ★.*
  ★★: GENERALLY MOVES FASTER THAN ★.
  This classification shall be adjusted by each distributor because it depends on model number, temperature, humidity, etc.
- *Parts whose parts numbers are omitted are subject to being not supplied.*

- **Parts List**

Mark	No.	Part No.	Description
	1.	BMN30P080FZK	Screw
	2.	CNB-832	Case
	3.	CMZ30P100FZK	Screw
	4.	CNR-240	Heat Sink
	5.	BMZ30P080FZK	Screw
	6.	BMZ30P060FZK	Screw
	7.	BMZ30P040FMC	Screw
	8.		Chassis
	9.	CDF-888	Connector
	10.	CDF-887	Connector
	11.	CDK-098	Cord
	12.	CDF-889	Connector
	13.		Plate
	14.	BMZ30P060FMC	Screw
	15.	CKS-267	Plug (2P)
★★	16.	TC9178F	IC (IC4)
★★	17.	TC9179F	IC (IC6)
★★	18.	HSH-156	Switch (LEVEL)
	19.	CKS-271	Plug (6P)
	20.	CKS-268	Plug (3P)
	21.	CKS-273	Plug (8P)
	22.	HKS-197	Connector (8P)
	23.	CWX-559	Signal Processor Unit
	24.	CDF-890	Connector
	25.	BMZ30P080FMC	Screw
	26.		Bracket
	27.		Bracket
	28.		Bracket
	29.	CNM-030	Spacer
★★	30.	NJM78M05A	IC (IC1)
	31.	CNM-783	Bush
	32.	BMZ30P060FMC	Screw
★★	33.	NJM78M12A	IC (IC9)
★★	34.	NJM79M12A	IC (IC10)
★★	35.	2SC2654	Transistor (Q152)
	36.	CKS-269	Plug (4P)
	37.	CKS-272	Plug (7P)
	38.	CDF-795	Connector (6P)
	39.	CBA-124	Screw, M3 x 5
★★	40.	2SC1847	Transistor
★★	41.	2SA886	Transistor
	42.		Bracket
★★	43.	µPC494C	IC (IC50)
	44.		Cushion
	45.	VACANT	
	46.	CCL-133	Feed through Capacitor
	47.	CWX-620	Servo Unit
	48.		Shield
	49.	VACANT	
	50.		Bracket
	51.	BBN30P080FZK	Screw

• Parts List

NOTE:

- *For your parts Stock Control, the fast moving items are indicated with the marks ★★ and ★.*
  ★★: GENERALLY MOVES FASTER THAN ★.
  This classification shall be adjusted by each distributor because it depends on model number, temperature, humidity, etc.
- *Parts whose parts numbers are omitted are subject to being not supplied.*

Mark	No.	Part No.	Description
	1.	CNN-279	Spacer
	2.	CNG-596	Holder
	3.	CNG-597	Holder
	4.	CNR-224	Magnet
	5.	CNW-924	Clamper
	6.	CNN-280	Felt
	7.	BMZ20P040FMC	Screw
	8.	CXD-367	Plate Unit
	9.	CBH-824	Spring
	10.		Stopper
	11.	HBA-173	Screw, M2 x 2
	12.	CXD-363	Arm Unit
	13.		Lever Unit
	14.	YE15FUC	E-ring
	15.	CNW-916	Lever
	16.	CLB-587	Collar
	17.		Arm Unit
	18.	YE20FUC	E-ring
	19.	CXD-360	Plate Unit
	20.	CNY-032	Holder
	21.	BMZ20P030FMC	Screw
	22.	CNW-912	Bearing
	23.	CNW-913	Bearing
	24.		Shaft
	25.		Arm
	26.	CBH-862	Spring
	27.	CBH-825	Spring
	28.		Arm
	29.		Lever Unit
	30.	BMZ26P040FMC	Screw
	31.	CLB-666	Collar
	32.	CXD-364	Arm Unit
	33.	CLB-586	Roller
	34.		Bracket
	35.	HEF-102	Clamper
	36.	BMZ26P030FMC	Screw
	37.		Lever
	38.		P.C. Board
★★	39.	CSN-094	Switch
	40.	CBA-172	Screw, M1.7 x 5.5
	41.	CNN-276	Sheet
	42.	CXD-366	Tray Unit
	43.		Holder
	44.	CLB-584	Collar
	45.	CBA-182	Screw, M2.6 x 5
	46.	CNW-926	Bush
	47.		Bracket
	48.	HBF-145	Washer
	49.	CNW-917	Gear
	50.	CBF-139	Washer
	51.	CNW-918	Gear
	52.	CNW-920	Gear
	53.	CNW-919	Gear
	54.		Bracket
★★	55.	CXD-696	Motor Unit (LOADING)
	56.	CBA-097	Screw, M2.3 x 4
	57.		Chassis Unit
	58.		P.C. Board
	59.	CDF-897	Connector
	60.	BMZ20P080FMC	Screw
	61.	CNW-909	Pulley
	62.	CLB-670	Collar
	63.	CBH-823	Spring
	64.	CXD-374	Arm Unit
	65.	BMZ26P060FMC	Screw
	66.	CNW-914	Spacer
	67.		Chassis
	68.		Rivet
	69.	CDF-899	Connector
	70.	VACANT	
	71.	CXD-773	Bracket Unit
	72.	BMZ20P025FMC	Screw
	73.	CBH-882	Spring
★★	74.	CXM-203	Motor (CARRIAGE)
★★	75.	CXM-405	Motor (SPINDLE)
	76.	iMZ26P060FMC	Screw
	77.		Shaft
★★	78.	CNT-110	Belt
	79.	CXD-373	Pulley Unit
	80.	CNW-911	Bearing
	81.		Shaft
	82.	CBL-227	Spring
	83.	CNR-223	Housing
	84.	CNW-925	Rack
	85.	BMZ30P040FMC	Screw
	86.	PMA30P050FMC	Screw
	87.	CBA-171	Screw, M3 x 4
	88.		Spacer
	89.	CNW-915	Spacer
	90.	CBL-228	Spring

Mark	No.	Part No.	Description
	91.	CGM-001	Pickup
	92.	CNL-665	P.C. Board
	93.	iMZ20P040FMC	Screw
	94.		P.C. Board
	95.	CLB-744	Collar
	96.	CBH-883	Spring
	97.	CEF-008	Clamper
	98.	CXD-375	Mechanism Unit

13. ELECTRICAL PARTS LIST

NOTE:

When ordering resistors, first convert resistance values into code form as shown in the following examples.

Ex. 1 When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J = 5%, and K = 10%).

560Ω 56×10^1 561 .... RD1/4PS 5 6 1 J
47kΩ 47×10^3 473 .... RD1/4PS 4 7 3 J
0.5Ω 0R5 .... RN2H 0 R 5 K
1Ω 010 .... RS1P 0 1 0 K

Ex. 2 When there are 3 effeictive digits (such as in high precision metal film resistors).

5.62kΩ 562×10^1 .... RN1/4SR 5 6 2 1 F

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- *Parts whose parts numbers are omitted are subject to being not supplied.*

Main Unit (CWX-561)

MISCELLANEOUS

Mark	Symbol & Description	Part No.
★★	IC1	TC40H004F
★★	IC2	NJM4558M
★★	IC3	KHA303
★★	IC4	KHA304
★★	IC5	NJM2904D
★★	IC6	PD6029
★★	IC7	M54546L
★★	IC8	TC4001BF
★★	IC9	NJM2903M
★★	IC101	TC4066BP
★★	IC102 – IC104	TA75558P
★★	Q1 – Q9, Q11 – Q13, Q101, Q102, Q107, Q108 Chip Transistor	2SC2712-LG or 2SC2712-LY
★★	Q10 Chip Transistor	2SA1162-SG or 2SA1162-SY
★★	Q14, Q21 – Q26, Q203 Chip Transistor	UN2211
★★	Q15	2SD1226M
★★	Q103, Q106 Chip Transistor	UN2111
★★	Q201	2SC1847
★★	Q202	2SA683
★	D1, D202, D205 Chip Diode	MA3075
★	D2, D3, D5 – D8, D101, D102 Chip Diode	MA151A
★	D9 Chip Diode	MA153
★	D10 Chip Diode	MA151WK
★	D103, D104	MTZ6R2
★	D201, D203	SIB01-02
	L201 Coil, 0.37mH	CTF-235
	L202 Ferri-Inductor, 15μH	CTF-078
	L203 Transformer	CTX-073
★★	VR1, VR2 Semi-fixed, 2.2kΩ (B)	CCP-374
★★	VR3 Semi-fixed, 47kΩ (B)	CCP-443
★★	VR4 Semi-fixed, 10kΩ (B)	CCP-439
★★	VR101, VR105 Semi-fixed, 4.7kΩ (B)	CCP-347
★★	VR102 Semi-fixed, 330kΩ (B)	CCP-358
★★	VR103 Semi-fixed, 4.7kΩ (B)	CCP-347
★★	VR104 Semi-fixed, 10kΩ (B)	CCP-349
★	TH1	CCX-010

Mark	Symbol & Description		Part No.
	X1	Ceramic Oscillator (4MHz)	CSS-030
	X2	Buzzer	CPV-031
★	ZNR201		ERZ-M10DK220

RESISTORS

Mark	Symbol & Description	Part No.
	R1 – R54, R57, R58, R61 – R68, R71 – R87, R89 – R97, R101 – R111, R114 – R130, R133 – R141, R201, R202, R204 – R209 Chip Resistor	RS1/8S □□□J
	R55, R56	RN1/2P □□□JL
	R70	RS1P □□□JL
	R69	RS1/2P □□□JL

CAPACITORS

Mark	Symbol & Description	Part No.
	C1, C7, C9 – C11, C13, C20, C24, C27 Chip Capacitor	CKSYF473Z50
	C2, C45, C46, C75	CEA220M16LS
	C3, C29, C30 Chip Capacitor	CKSYF224Z25
	C4, C5, C12, C17 Chip Capacitor	CKSYB473K25
	C6, C25, C121, C122 Chip Capacitor	CCSCH220J50
	C8, C21, C26, C74	CEA010M50LS
	C14, C22, C23, C72, C73 Chip Capacitor	CCSCH101J50
	C15, C16, C77 Chip Capacitor	CCSSL332J50
	C18	CEAR47M50LS
	C28, C41, C42, C44, C47, C71, C76, C78, C79 Chip Capacitor	CKSYF473Z50
	C43	CEA470M16LS
	C48, C201, C205	CCG-081
	C80, C103 Chip Capacitor	CCSSL222J50
	C101, C102 Chip Capacitor	CEA470M16LS
	C104, C105, C113, C114, C119, C120 Chip Capacitor	CKSYF473Z50
	C106	CQMA104J50L
	C107, C123 Chip Capacitor	CCSCH330J50
	C108, C109 Chip Capacitor	CKSYF224Z25
	C110	CQMA823J50L
	C111 Chip Capacitor	CCSSL122J50
	C112 Chip Capacitor	CCSSL332J50
	C115	CEA3R3M50LS
	C116 Chip Capacitor	CCSCH152J50
	C117	CQMA103J50L
	C118 Chip Capacitor	CCSCH271J50
	C202, C206, C208, C214 – C216 Chip Capacitor	CKSYF473Z50
	C203, C207	CEA471M16L2

Mark	Symbol & Description		Part No.
	C204		CEA100M16LL
	C209		CEA101M16LL
	C210		CSYA1R5M250S
	C211		CEA330M35L2
	C212	Chip Capacitor	CKSYF224Z50
	C213		CEA330M25L2

Display Unit (CWX-562)

MISCELLANEOUS

Mark	Symbol & Description		Part No.
★★	IC301		PD7005
★	D301 – D310	LED	BG5724K
★★	S1 – S9	Switch	CSG-212
★		Display	CP2131GLR

CHIP RESISTORS

Mark	Symbol & Description	Part No.
	R301 – R329	RS1/8S □□□J

CHIP CAPACITORS

Mark	Symbol & Descriptions	Part No.
	C301	CKSYF473Z50
	C302	CCSCH101J50

Servo Unit (CWX-620)

MISCELLANEOUS

Mark	Symbol & Description	Part No.
★★	IC1, IC11	NJM78M05A
★★	IC2	PD3036
★★	IC3	PD8010
★★	IC4	NJM2903S
★★	IC5, IC7, IC8	TA75558S
★★	IC6	TC4066BP
★★	IC9	NJM78M12A
★★	IC10	NJM79M12A
★★	IC12	NJM79L05A
★★	IC50	μPC494C
★★	Q1 Chip Transistor	UN2211
★★	Q2 Chip Transistor	UN2111
★★	Q3, Q7 – Q9, Q13 – Q22, Q25, Q26, Q28, C29	DTC124ES
★★	Q4, Q12	2SA683
★★	Q5, Q31	2SC2458
★★	Q6	DTC144WS
★★	Q10	2SA1048
★★	Q23, Q27, Q30, Q151	DTA124ES
★★	Q32, Q34, Q36, Q38	2SC1847
★★	Q33, Q35, Q37, Q39	2SA886
★★	Q40	2SA798
★★	Q152	2SC2654
★	D1	VACANT
★	D2, D4, D151 Chip Diode	MA151K
★	D5, D7 Chip Diode	MA151WK
★	D152 – D155	11DQ05FC or 11DQ06FC
★	ZD1 Chip Diode	MA3056
★	ZD2	RD20EB1 or RD20EB2 or MTZ20A or MTZ20B
★	ZD151, ZD152	RD20EB3 or RD20EB2
	L1 Coil, 5.6 μH	CTF-234
	L2, L3 Coil, 100 μH	CTF-232
	L4, L5 Coil	CTF-233
	T1 Transformer	CTH-085
	T2 Transformer	CTH-086
	T3 Transformer	CTH-084
★	TH1 Posistor	CCX-017
	X1 Ceramic Oscillator (4 MHz)	CSS-030

RESISTORS

Mark	Symbol & Description	Part No.
	R1 – R13, R15 – R54, R56 – R95, R97 – R100, R151 – R163, R165, R166, R168, R170 Chip Resistor	RS1/8S □□□J
	R164	RD1/4PM □□□J
	R167	RD1/4VM □□□J
	R169 0.1Ω (2W)	CCN-135

CAPACITORS

Mark	Symbol & Description	Part No.
	C1, C2	CEA100M25LS
	C2, C4, C5, C33 – C40	CEA010M50LS2
	C6, C7 Chip Capacitor	CCSSL101J50
	C8	CEA471M10L2
	C9 – C11, C13 – C15, C19, C20, C23, C41 Chip Capacitor	CKSYF103Z50
	C16, C17	CEA470M16LS
	C18	CQMA104J50L
	C22, C26 Chip Capacitor	CCSSL151J50
	C24, C27 Chip Capacitor	CKSYF224Z50
	C28	CEA101M16L2
	C29, C30 Chip Capacitor	CKSYF103Z50
	C31, C32	CEA470M25L2
	C42, C43 Chip Capacitor	CKSYB392K50
	C44	CKDYB102K50
	C45	CCDSL101J50
	C72	CCG-104
	C151, C154 Chip Capacitor	CKSYF473Z50
	C152, C153, C165, C166, C171, C172	CSYA1R5M250S
	C155	CEAUH471M25
	C156	CEA100M25LS
	C157	CQMA103J50L
	C158	CQSAH102J50
	C159, C161 – C164	CEAUH101M25
	C160	CEAUH331M50
	C167 – C170	CEAUH101M16
	C1000 Feed through Capacitor	CCL-133

Signal Processor Unit (CWX-559)

MISCELLANEOUS

Mark	Symbol & Description		Part No.
★★	IC1		KHA301
★★	IC2, IC7		NJM4558DD
★★	IC3		TD6315AP
★★	IC4		TC9178F
★★	IC5		HM6116ASP-20
★★	IC6		TC9179F
★★	IC8		TC4027BP
★★	IC9		TC4001BP
★★	IC10		NJM78L08A
★★	IC11		NJM79L09A
★★	IC12		TD6705AP
★★	IC13		NJM072S
★★	IC14, IC15	Filter	CWW-225
★★	IC16, IC17		TA75558S
★★	Q1 – Q3, Q5, Q6		2SC2458
★★	Q4, Q9		2SA1048
★★	Q7, Q8		2SD1012
★	D1, D3, D4, D6, D7	Chip Diode	MA151A
★	D2	Chip Diode	MA153
★	D5	Chip Diode	MA151WA
★	D8		KV1226Y
	L1, L2	Coil, 470 μH	CTH-063
	L3	Coil	CTA-070
	F1	SAW Resonator	F1383K
	X1	X'tal (8.4672 MHz)	CSS-040
★★	VR1, VR2	Semi-fixed, 10kΩ (B)	CCP-349
★★	S1	Switch (LEVEL)	HSH-156

RESISTORS

Mark	Symbol & Description		Part No.
	R1 – R44, R51 – R78, R87 – R94	Chip Resistor	RS1/8S □□□J
	R79 – R86		RN1/4PQ □□□F

CAPACITORS

Mark	Symbol & Description		Part No.
	C1, C2, C58, C66		CEA010M50LS2
	C3, C4, C14, C27		CEA100M25LS
	C5		CEA470M25L2
	C6, C21, C59, C65		CEA470M16LS
	C7, C8, C11, C15 – C18, C22, C23,		CKSYF103Z50
	C26	Chip Capacitor	
	C9		CQMA822K50L
	C10	Chip Capacitor	CCSCH151J50
	C12	Chip Capacitor	CCSCH331J50
	C13	Chip Capacitor	CCSCH221J50
	C19		CQMA103J50L
	C20	Chip Capacitor	CCSSL681J50
	C24, C25, C69, C70	Chip Capacitor	CCSCH150J50
	C28 – C30, C36, C51, C52, C56, C62, C67, C68	Chip Capacitor	CKSYF103Z50
	C31, C33, C35	Chip Capacitor	CKSYB332K50
	C32, C34	Chip Capacitor	CKSYB103K50
	C53	Chip Capacitor	CCSSL470J50
	C54, C55	Chip Capacitor	CCSSL050C50
	C57	Chip Capacitor	CKSYB102K50
	C60, C63		CQSAH102J50
	C61, C64		CCDSL150J50
	C71 – C74, C77 – C79	Chip Capacitor	CKSYF103Z50
	C75, C76		CQMA153J50L
	C80, C81		CEA330M16L2

Pre Amp Assy (CWK-384)

MISCELLANEOUS

Mark	Symbol & Description		Part No.
★★	IC1		M5218L
★★	IC2		TA75558S
★★	Q1, Q2		2SA1048L-GR or 2SA933SLN-S
★★	Q3		2SB647-C
★★	Q4		2SC2458 or 2SC1740S
★★	Q5		2SD468-C
★★	Q6		2SC1815
★★	Q7		2SA1015
★	D1 – D8		1SS133 or 1SS176
★	D9		HZ9A or RD8R2EB2 or MTZ8R2B
★	D10		HZ6A or RD5R6EB or MTZ5R6EB
★	D11, D12	LED	BG5724K
★★	VR1	Volume, 50kΩ (W), 20kΩ (A) (VOLUME, BALANCE)	CCS-433
★★	VR2	Volume, 50kΩ (B) (BASS, TREBLE)	CCS-432

RESISTORS

Mark	Symbol & Description	Part No.
	R1 – R39, R41 – R45	RD1/6PS □□□J
	R101	RD1/4PM □□□J

CAPACITORS

Mark	Symbol & Description	Part No.
	C1, C2, C15 – C20	CEANL100M16LL
	C3, C4, C13, C14	CCDSL330J50L
	C5, C6	CEA100M16NPLL
	C7 – C10	CQMA182J50L
	C11, C12	CQEA333J50
	C21, C22	CEA470M16L2
	C23	CEA471M10L2
	C24	CEA221M10L2
	C25	CEA221M16L2
	C26	CEA101M16LL
	C27	CEA470M16LS
	C28	CQEA473J50

Miscellaneous Parts List

Mark	Symbol & Description		Part No.
		Pickup	CGM-001
★★	M1	SPINDLE Motor	CXM-405
★★	M2	CARRIAGE Motor	CXM-203
★★	M3	Motor Unit (LOADING)	CXD-696
★★	S10 – S13	Switch (FRONT, HOME, INTER LOCK, DISC DETECT)	CSN-094

14. PACKING METHOD

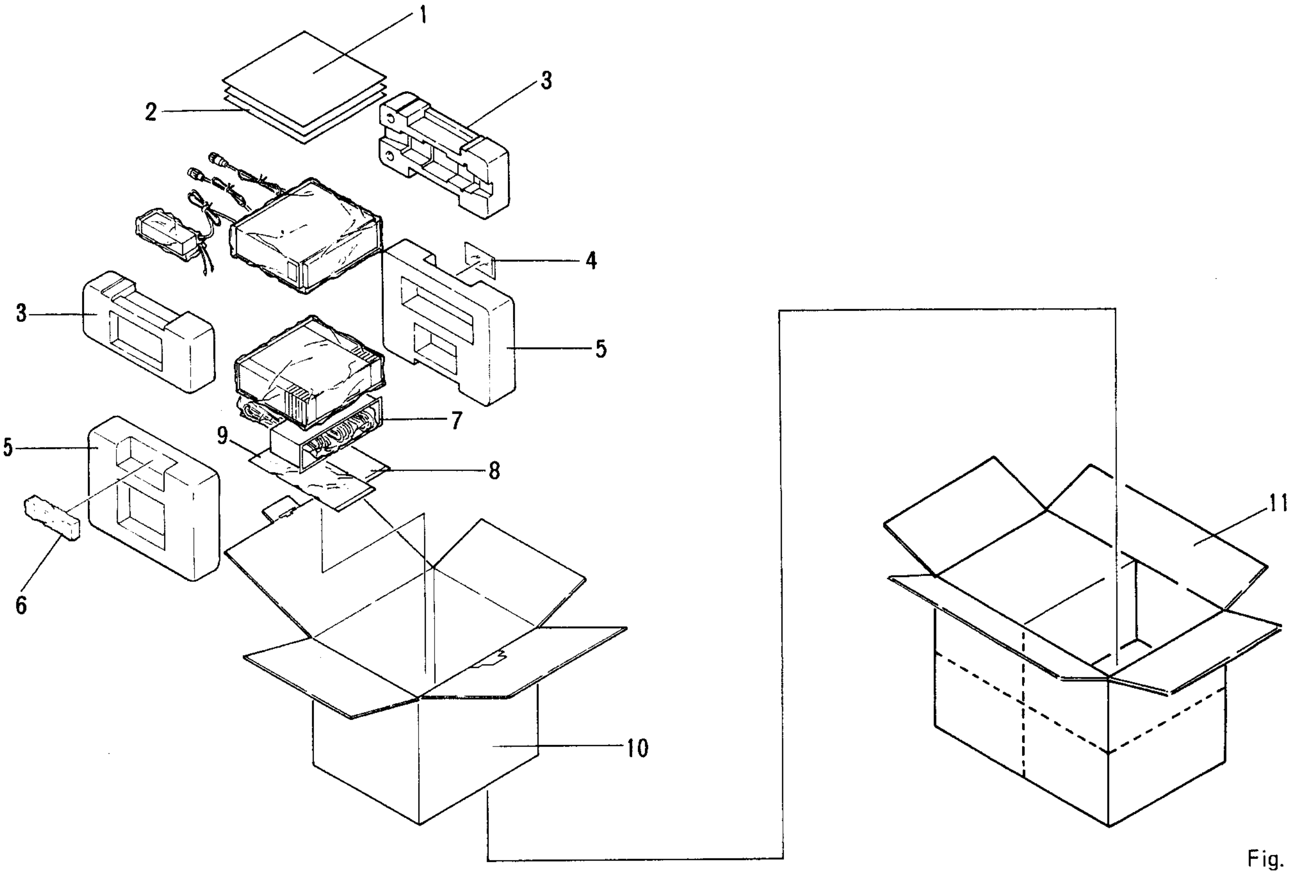


Fig. 77

• Parts List

Mark	No.	Part No.	Description
	1.	CRB-526	Owner's Manual (CDX-P1/US) (English)
		CRD-551	Owner's Manual (CDX-P1/EW) (English, French, German, Spanish)
		CRD-553	Owner's Manual (CDX-P1/ES) (English, French, Spanish, Arabic)
	2.	CRD-552	Owner's Manual (CDX-P1/EW) (Swedish, Norwegian, Dutch, Italian)
	3.	CHF-045	Styrofoam
	4.	CEA-225	Screw Assy
	4-1.	B10-819-A	Screw, M3 x 4
	4-2.	B20-004	Washer, 4ϕ
	4-3.	B20-223-F	Pin, 3 x 30
	4-4.	B30-174-A	Screw, M5 x 16
	5.	CHD-960	Styrofoam
	6.		Bracket Assy
	6-1.	CNE-510	Bracket
	6-2.	CNM-667	Fastener
	7.	CNG-223	Holder
	8.		Panel Assy
	8-1.	CNB-793	Panel
	8-2.	CNW-757	Holder
	9.	CEA-885	Accessory kit
	9-1.	CDE-437	Cord
	9.2	CNF-111	Strap
	9-3.	CNF-382	Lever
	9-4.	CNW-642	Holder
	9-5.		Screw kit
	9-5-1.	CBA-028	Screw for Strap
	9-5-2.	NF40FMC	Nut
	9-5-3.	NF50FMC	Nut
	9-5-4.	PMB50Y160FMC	Screw
	9-5-5.	WS40FMC	Washer
	10.	CHF-068	Carton (CDX-P1/US, ES)
		CHF-070	Carton (CDX-P1/EW)
	11.	CHF-069	Contain Box (CDX-P1/US)

88

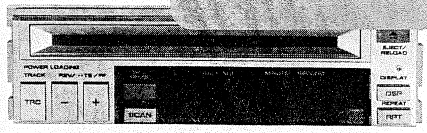
SCHALTUNGSDIENST LANGE BERLIN
PIONEER BELEGEXEMPLAR

LFD.NR.: 1013

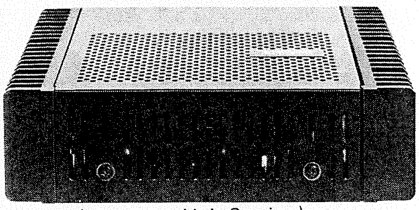
Service Manual

XP 88

CIRCUIT DESCRIPTIONS



(Player Section)



(Hideaway Unit Section)

ORDER NO.
CRT-487-0

COMPONENT CAR STEREO COMPACT DISC PLAYER

CDX-1 US,ES,EW

- For the repair and adjustment, please refer to the CDX-1 service manual (CRT-483, CRT-484).

CONTENTS

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4. THE CD PLAYER CONTROL SYSTEM 24
5. MICROCOMPUTER SYSTEM OPERATIONS 26
6. SERVICING INFORMATION 35

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1013

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SPECIFICATIONS

General

System	Motor vehicle compact disc digital audio system
Disc	Diameter: 120 mm Thickness: 1.2 mm Maximum playing time: Over 60 minutes (stereo) Linear velocity: 1.2～1.4 m/sec. Rotation direction: Counterclockwise
Signal format	Sampling frequency: 44.1 kHz Number of quantization bits: 16; linear Transmission bit rate: 4.3218 Mbit/sec. Modulation system: EFM Error correction system: CIRC Pre-emphasis: 50/15μsec.
Laser	Semiconductor laser: wavelength 780 nm
Power requirements	14.4V DC (10.8～15.6V possible)
Power consumption	18W
Weight	Player section: 2.1 kg Hideaway unit section : 1.7 kg
Dimensions	Player section: 180(W)x50(H)x165(D) mm Hideaway unit section: 180(W)x50(H)x165(D) mm

Audio

Frequency characteristics	5～20,000 Hz (±1 dB)
Signal-to-noise ratio	90 dB (1 kHz) (IEC-A network)
Dynamic range	90 dB (1 kHz)
Wow and flutter	Below measurement range
Distortion factor	Below 0.005% (1 kHz, 0 dB)
Output voltage	280 mV (1 kHz, 0 dB) (when level switching High) 140 mV (1 kHz, 0 dB) (when level switching Low)
Number of channels	2 (stereo)

Note:
Specifications and the design are subject to possible modification without notice due to improvements.

1. OUTLINE OF COMPACT DISC PLAYER

The CDX-1 is CD (Compact Disc) player system with compact pickup unit developed exclusively for car CD players.
The configuration of this CD player is as follows:

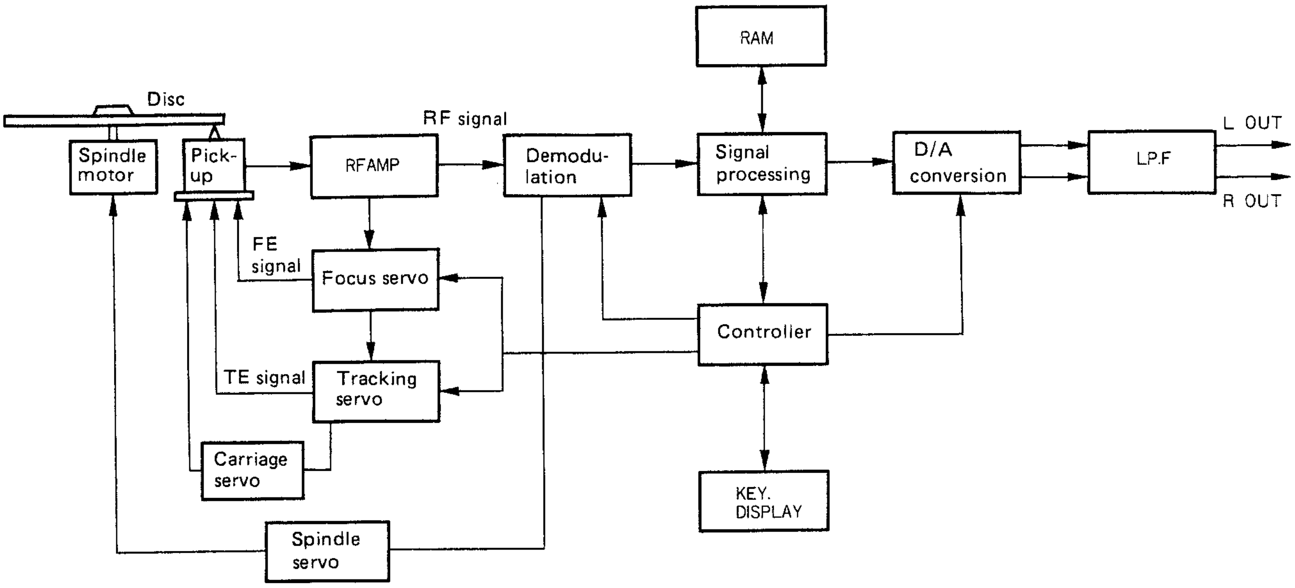

RAM
Disc
RF signal
Spindle motor
Pick-up
RFAMP
Demodulation
Signal processing
D/A conversion
L.P.F
L OUT
R OUT
FE signal
Focus servo
TE signal
Tracking servo
Controller
Carriage servo
KEY. DISPLAY
Spindle servo

Fig. 1

The FE (Focus Error) signal and the TE (Tracking Error) signal are derived from the RF signal generated at the pickup unit. The FE signal controls the focus actuator which focuses the pickup unit. The TE signal controls the tracking actuator which accurately traces the tracks on the disk surface. A microcomputer controls these signals, the carriage motor which moves the pickup unit, and the spindle motor which turns the disc.

The following sections describe the pickup and servo systems, RF signal processing, and the microcomputer control system and its operation.
Refer to the P-D1 service manual for a detailed description of the optical system and an explanation of the operating principle of the compact disc.

2. EXPLANATION OF THE PICKUP AND SERVO SYSTEM

2.1 PICKUP

Fig. 2 shows the pickup unit configuration diagram.

The pickup employs a laser diode (LD) that generates a laser beam with a wavelength of approximately 780 mm. The RF signal, the FE (Focus Error) signal and the TE (Tracking Error) signal are derived from this laser beam.

As shown in Fig. 2 (the optical system), a diffused laser beam is emitted from the LD, and is then made parallel by a collimator lens. This parallel beam is sent through a beam splitter, a reflection prism, and then through a quarter-wavelength plate. The objective lens then focuses the beam on the disc surface.

The beam is flashed onto a row of pits on the disc surface, and then reflected back through the objective lens. Then it passes through the quarter-wavelength plate the reflection prism, and finally goes through the beam splitter again. The LD emits a straight polarized beam which is then changed to a circular, polarized beam by passing through the quarter-wavelength plate. After the beam is reflected off the disc plane, it goes back through the quarter-wavelength plate and is changed back into a straight polarized beam.

The polarity of the returning beam is 90 degrees out of phase with the outgoing beam. The beam is reflected off the disc plane, goes back through the quarter-wavelength plate, and is reflected off the beam splitter. It then goes through a critical angle prism and finally reaches the four-segment PD (Photo Detector).

The FE signal is detected by the critical angle prism and the four-segment PD.

The TE signal is generated using a signal detected from a single beam; the method is called the heterodyne method. This method makes use of the distribution of the beam diffracted from the pits as it changes in relation to the radial position of the beam spot and the pits. The TE signal is detected by sampling and holding the DL signal of the RF signal cross point, the phase of which is detected by combining elements appearing diagonally on the four-segment PD.

The pickup unit objective lens moves along the optical and radial axes of the pickup system in order to control the beam spot focus and tracking. The objective lens is supported by two parallel springs and moves along the optical axis. This lens also moves parallel to the radial axis without inclining towards the optical axis because the two parallel springs are supported by two additional springs set in an inverted "v" configuration. Therefore, the objective lens is driven in both directions with the two sets of coils installed on both sides of the lens.

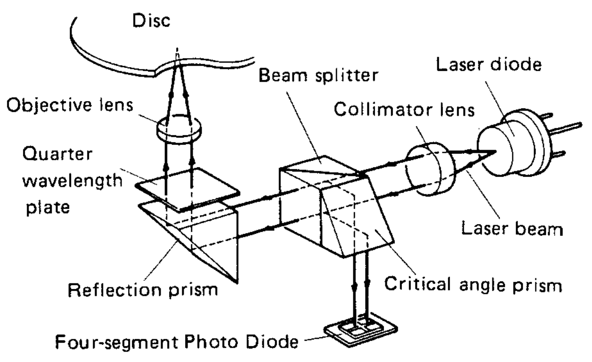


Fig. 2

2.2 APC CIRCUIT

The output characteristics of the laser diode are greatly affected by changes in temperature. The beam output must be kept constant at all temperatures in order to accurately read the information recorded on the disc. An MD (Monitor Diode) has been built into the pickup for the purpose of monitoring the quantity of beam output. The beam output from the LD is kept constant by applying negative feedback from the current (detected by the MD) to the LD drive circuit.

The current detected by the MD is input into the IC5(2/2) inverted input terminal after being converted into voltage by R61 and then amplified 40 times by IC5(1/2). The voltage, after being divided by R65 and VR4, is input into the IC5(2/2) non-inverted input terminal as the standard voltage. IC5 amplifies the difference between the two input voltages and that output current is then amplified by Q15 to activate the LD.

VR4 controls the beam intensity which is adjusted to 0.25 mW and projected into the objective lens.

The APC circuit is controlled by the a microcomputer, and when the microcomputer LD signal is "H," the current stops flowing to the LD. The LD can easily be damaged by surge currents or static electricity. To protect the LD, C45 to C48 have been placed on the power supply line, and a diode and capacitor have been inserted into the pickup unit.

2.3 PRE-AMPLIFIER

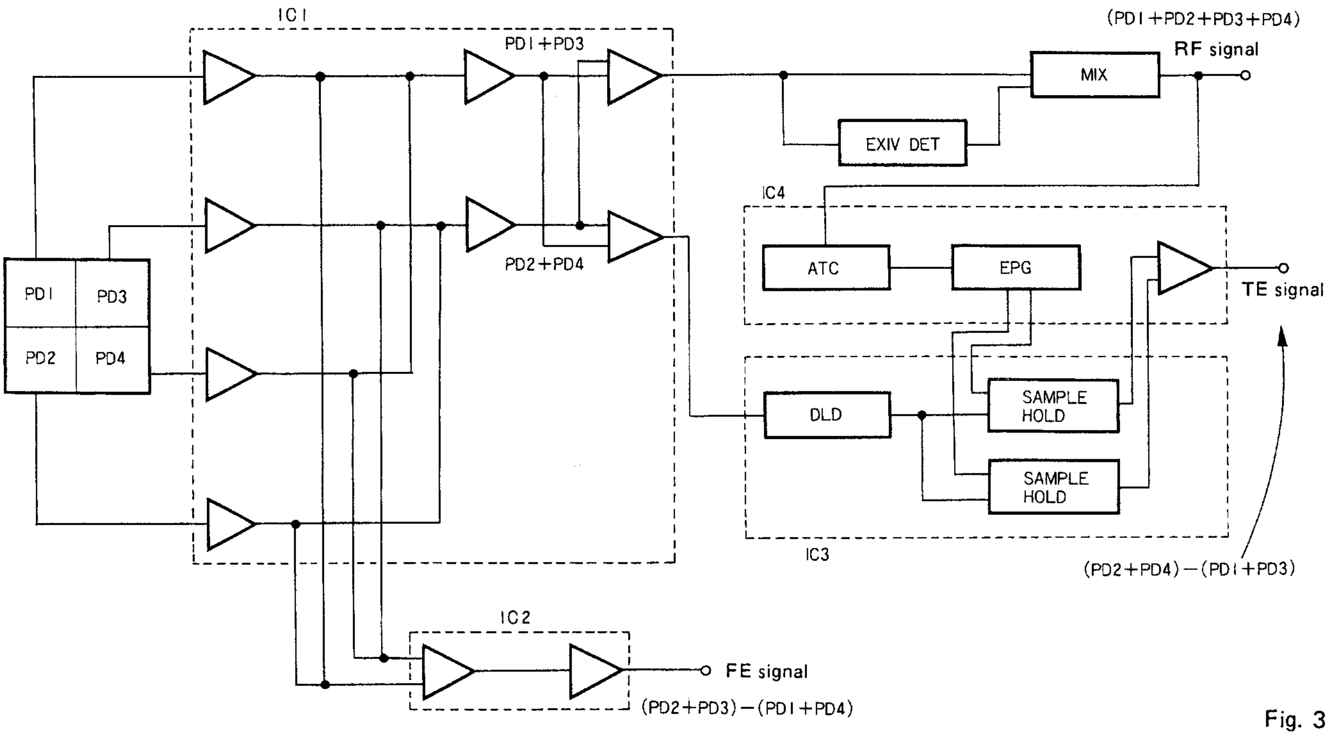


Fig. 3

The pre-amplifier generates the RF, TE and FE signals by amplifying and then adding/subtracting the output from the pickup unit four-segment PD.

Fig. 3 shows the block diagram for the pre-amplifier. The output current from the four-segment PD in the pickup unit is converted to voltage by IC1. After this, the FE signal is obtained by computing (PD2+PD3) – (PD1+PD4). When the objective lens is closer to the disc than the focal point is, the FE signal generates negative output: if the lens is farther from the disc, than the focal point, the FE signal generates positive output. IC2 performs the necessary computations and amplification for these functions.

The RF signal can be obtained by computing (PD1+PD2+PD3+PD4). After the RF signal is combined by transistor amplifier (Q4 and Q5), it goes through an emitter follower circuit (Q6). Its voltage level is adjusted by VR2, and mixed with an envelope signal. The envelope detection circuit improves the data reading capability during dropouts, or while the pickup is crossing over the tracks during a search operation. Q11, D3, R34 and C16 compose a peak hold circuit. This circuit detects the upper envelope of the RF signal.

Q10, D2, R33 and C15, compose a bottom hold circuit: this circuit detects the lower envelope of the RF signal. The time constants of the peak hold and bottom hold circuits are set to follow the long-pit components of the RF signal and not to follow the short-pit components.

The output of the envelope detection circuit and the RF signal are combined by a Q12 base ground amplifier. The TE signal is obtained by sampling and holding the DL (Deagonal Line) signal taken at the zero cross point of the RF signal. The TE signal is obtained from the differencein signal strength between the two pairs of diagonally placed PDs. (PD2-PD4) – (PD1-PD3)

According to the block diagram, the RF signal (the signal combinedwith an envelope signal) is converted to a binary signal by the ATC (Auto Threshold Control) circuit. Then the EPG (Edge Pulse Generator) circuit converts the signal to positive and negative edge pulses and sends them to the sample hold circuit. The DL signal is sent to the sample hold circuit via the DLD (DL Delay) circuit which compensates for delay time. After this, the TE signal is obtained through differential amplification of the output from the sample hold circuits.

The ATC, EPG and differential amplifier circuits are contained in IC4 (hybrid IC), and the DLD and sample hold circuits are inside IC3 (hydrid IC).

VR3 adjusts the DC offset of the TE signal produced in the optical system and circuitry.

2.4 FOCUS CONTROL

● Outline

A lead or lag in the FE signal which is generated by the pre-amplifier is compensated for by IC104(1/2) after passing VR105 (gain level control). This signal operates the focus actuator (objective lens) in the pickup unit with the current drive circuit made up of IC104 Q38 and Q39. This is how the focus servo is controlled. Focus offset level control VR104 adjusts the shifting of the focus within the optical system or the circuitry of the pre-amplifier. When the power of the CD unit is turned on, the focus servo opens and the spring-supported objective lens is positioned at the mechanical center.

Upon receiving a command to activate the focus servo circuit, the lens is first pulled back and then pushed outward. When the lens passes by the focal point, an RF signal is generated. This activates the focus servo circuit. The FT (Focus Trigger) signal determines whether or not the focus servo circuit is properly activated: If this circuit is not activated within a certain period of time, the disc is automatically ejected.

Focus control circuit (MAIN UNIT, CWV-561 2/3)

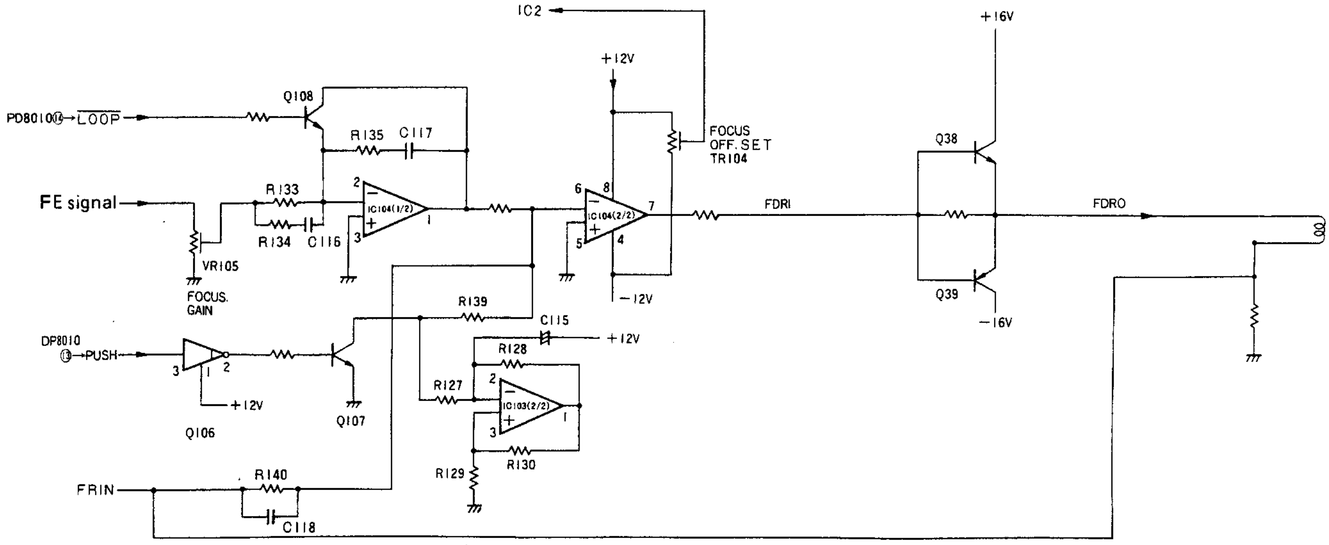

IC2
+16V
+12V
PD8010⑭→LOOP
Q108
R135
C117
FOCUS OFF.SET TR104
Q38
FE signal
R133
IC104(1/2)
R134
C116
VR105
FOCUS. GAIN
IC104(2/2)
FDRI
FDRO
-12V
Q39
-16V
R139
C115
+12V
DP8010 ⑬→PUSH
R128
R127
IC103(2/2)
Q106
Q107
R129
R130
FRIN
R140
C118

Fig. 4

● Focusing Circuit

After the PUSH signal is sent from the micro-computer, Q106 and Q107 turn off, which sends a charging current into C115 via R128. After the PUSH signal reaches the IC103(2/2) inverted input terminal, the signal becomes a triangular wave as shown in Fig. 5.

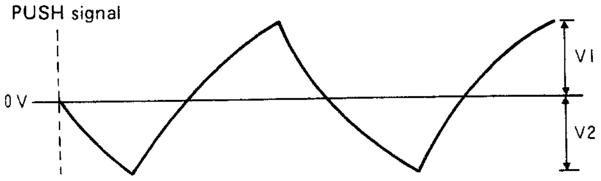


Fig. 5

The PUSH signal is then sent to IC104 (2/2) via R127 and R139, which in turn operate the actuator. When the voltage is negative, the actuator is driven away from the disc. The period is approximately 1.7 seconds.
R129 and R130 set V1 and V2 to approximately 2.2 V. When the power is turned on, 12V is momentarily sent to the inverted input terminal of IC103, and the output becomes −12V since the non-inverted terminal is the ground potential. Therefore, the actuator always starts from the pulling operation when the power is turned on. The In-focus detection takes place when the RF signal exceeds a certain level. After the detection, the LOOP signal becomes "L," and the servo loop closes. At this time, the push signal also becomes "L" and Q106 and Q107 turn on so that the signal does not go to IC104.

● Focus Servo Circuit

The FE signal generated in the pre-amplifier goes through VR105 and is sent to IC104(1/2). In this IC, the equalizer is constructed so that phase lead compensation (Poles 330 Hz, 4.4 kHz) is performed by C116, R133 and R134, and phase lag compensation (pole 72 Hz), by C117 and R135.
Q108 is incorporated in the negative feedback circuit to control the opening and closing of the servo. When the LOOP signal becomes "H," Q108 turns on which makes the IC104 gain zero, opening the servo loop.
The FE signal, after undergoing phase compensation, is converted into a current by Q38, Q39, and IC104 (2/2). By incorporating C118 and R140 into the feedback circuit, audible noise (5.9 kHz or more) generated by the actuator is reduced.

2.5 TRACKING CONTROL

● Outline

The Tracking Control controls the beam position in the radial direction of the disc so that the laser beam will accurately trace the tracks on the disc surface.

IC102(1/2) compensates for leads or lags in the TE signal which is generated by the pre-amplifier. In addition to this, R111 and C110 compensate for lags and IC102(2/2) compensates for leads. Signal gain is then adjusted by VR101. Then the current drive circuit consisting of IC103 (1/2), Q36 and Q37 starts the tracking actuator in the pickup unit. Finally, the tracking servo starts when the objective lens begins to move in the radial direction.

The tracking servo circuit is activated after the focus servo circircuit is activated. The tracking servo circuit activation, however, is controlled to reduce the pickup speed relative to the movement of the disc surface. There is also a jump circuit which accesses tracks randomly.

● Tracking Servo Circuit Activation

The tracking servo circuit activated after the focus servo circuit is activated. The tracks cross the beam spot one after the other due to their eccentricity. The activation becomes unstable if the tracking servo is closed when the relative cross-over speed between the beam spot and the tracks is great. If this gets bad enough, the tracking actuator starts to vibrate, making activation impossible. In order to avoid this, the tracking servo is designed to close only when the relative cross-over speed is low. It does this by detecting the disc movement with the RF and TE signals. The time charts for this operation are shown in Figs. 6 and 7.

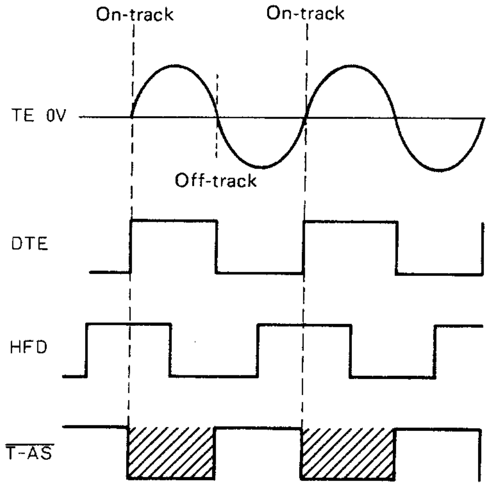
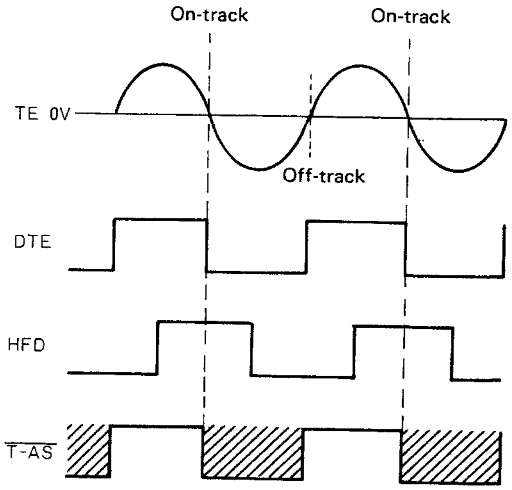


Fig. 6 Disc Shifting Toward Center.



(Shaded areas indicate servo loop closed)

Fig. 7 Disc Shifting Toward Outside Edge.

If the disc moves toward the outside edge because of eccentricity, the tracking servo loop is closed when the TE signal becomes positive. This condition is shown in figure 9. The DTE signal is obtained by converting the TE signal. The HFD signal is obtained by converting the RF signal; this signal turns to "H" in the "on track" vicinity, and to "L" in the "off track" vicinity. The $\overline{\text{T-AS}}$ (Tracking-Analog Switch) signal opens and closes the tracking servo. When this signal is "L" (shaded areas in the diagram), the servo is closed. As shown in the diagram, the servo loop is only turned on when the TE signal is positive. At this time the tracking actuator is activated to make the lens move back to the on-track position. That is, the difference in relative speed between the movement of the lens and the movement of the disc is reduced since the lens is moved in the same outward direction. Tracking servo circuit activation becomes possible when this process is repeated and the relative speed is reduced to a certain point.

The same principle allows tracking servo circuit activation to be performed for the movement of the lens in an inward direction. This reduces the amount of time required for tracking servo circuit activation.

At the time of activation, the TE signal frequency changes according to the degree of eccentricity. However, the timing of the $\overline{\text{T-AS}}$ signal can be delayed as much as the phase lead since the servo loop continues to open and close after undergoing phase lead compensation in R101, R102 and R103. Because of this, the phases of signals DTE and TE are matched at 1.1 kHz using high pass filters C11 and R58.

• Tracking Servo Circuit

The TE signal generated by the pre-amplifier is sent to IC102(1/2) via the analog switch, IC102(1/2). There are equalizers here for phase lead compensation (Poles 570 Hz, 10.5 kHz) made up of C103, R101 and R102, and for phase lag compensation (Poles 4.9 Hz, 59 Hz, 465 Hz) made up of C106, R109 and R110. This output is then sent to IC102(2/2). There are also equalizers for second stage phase lag compensation (10 Hz, 52 Hz, 4.4 kHz when the pole band is narrow, and 8.6 Hz, 264 Hz when the band is wide) and second stage phase lead compensation (Poles 1.1kHz, 1.8kHz).

The analog switch IC101 is set up by input to IC102(1/2) to open and close the servo loop. When the $\overline{\text{T-AS}}$ signal is "H," and Q103 is off, the analog switch impedance becomes high, and the loop opens.

After VR101 has adjusted the phase compensated TE signal, that signal then undergoes current conversion at IC103(1/2), Q36 and Q37 and operates the actuator. Feedback circuit IC103 contains C107 and R124: it reduces audible noise (16 kHz or more) created by the actuator.

The second stage equalizer switches bands as follows: The band is divided into two stages, wide and narrow. The bands are switched according to the conditions. The wide band is used during tracking servo circuit activation or jump operations, and the narrow band is used during normal playing.

VR103 functions to cut off the off-set voltage generated inside the circuit and sets the actuator drive current to zero when the tracking servo is open.

• Jump Control circuit

In the final stage of locating the target address during a search operation, jump operations are executed in the pause mode. A microcomputer generates a signal which controls the tracking servo. The tracking servo moves the beam spot in or out one track at a time in response to each jump command received from the microcomputer. The microcomputer controls the direction of the jump with "J+" and "J–" signals. It will move one track outward with a "jump forward" command, and one track inward with a "jump reverse" command. Figure 8 shows timing charts for signals during the Jump Forward Operation.

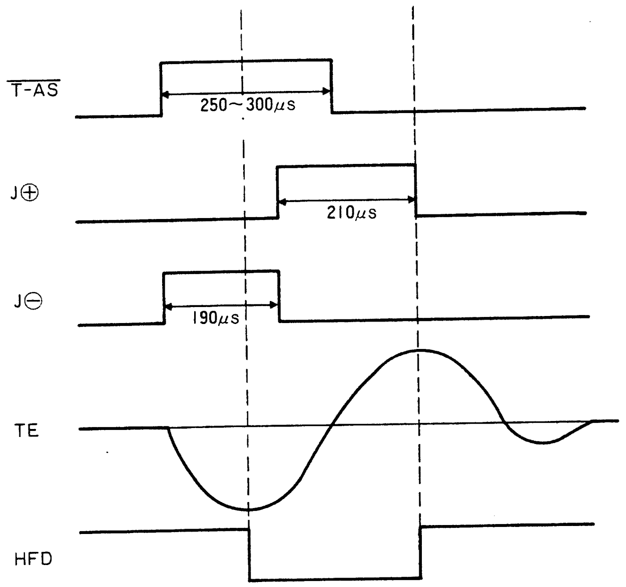


Fig. 8

At the start of the jump operation the $\overline{\text{T-AS}}$ signal is "H," and as soon as the tracking servo loop opens, the "J–" signal turns to "H" and the Q102 base emitter voltage is applied to IC103 via the IC101 analog switch. Then a current flows into the tracking actuator to move the beam spot outward. As the beam spot moves outward, the TE signal moves in a negative direction until it reaches the negative peak. When the beam spot gets half way to the adjoining outside track (approximately 0.8mm above the track), it switches from negative to positive. At this point, the $\overline{\text{T-AS}}$ signal turns to "L" and closes the servo loop. The beam spot is then drawn into the next track.

However, when the TE signal is crossing zero, the actuator continues to move outward and the beam spot can be pulled into the track even after the servo loop is closed. In order to keep the beam spot from skipping the next track, the J– and J+ signals are made "L" and "H," repectively – before the TE signal switches from negative to positive – to produce braking force and thus to facilitate beam spot tracking. In order to further reduce the amount of overshoot even after the adjustment, the pulse width of the "J+" signal is made wider than that of the "J–" signal, to generate a decelerating force greater than the accelerating force. A microcomputer sets these pulse widths.

With jump reverse, the "J+" signal becomes "H" to move the signal actuator inward while the "J–" signal is used to provide the decelerating force. VR102 adjusts the $\overline{\text{T-AS}}$ signal time during jumping to the 250 – 300 μsec range.

Tracking Control Circuit (MAIN UNIT CWX-561 2/3)

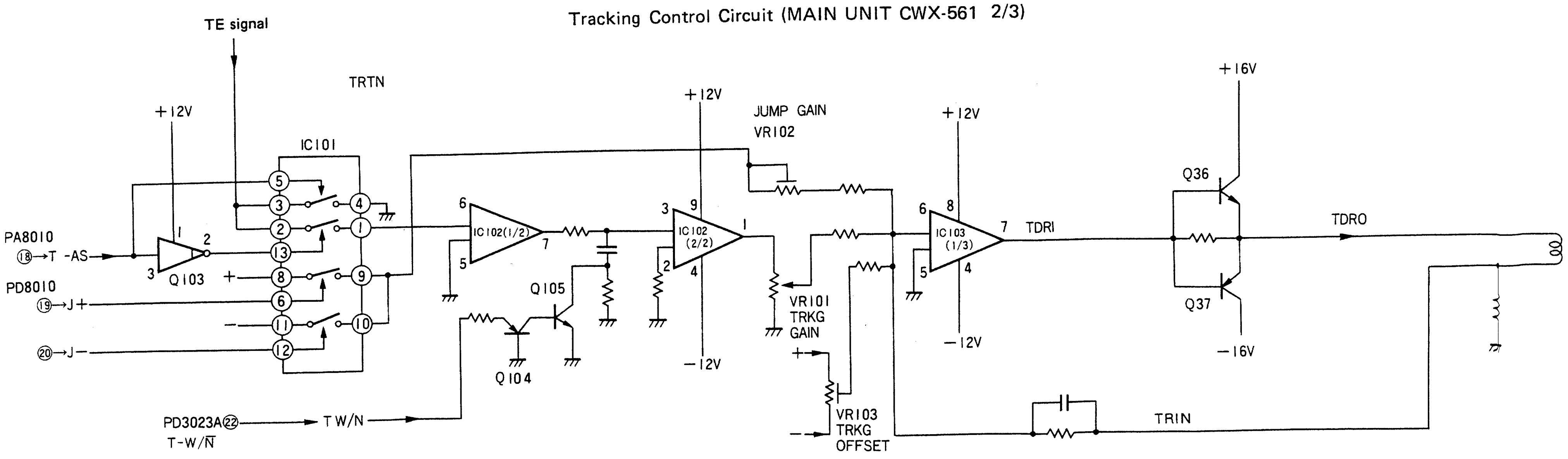


Fig. 9

2.6 CARRIAGE CONTROL CIRCUIT

The Carriage Control Circuit moves the pickup inward and outward in the radial direction on the disc surface.

For normal playing, the beam moves outward, and traces the tracks on the disc surface. The actuator, however, can only move about 0.4 mm. When the drive current of the actuator increases, this circuit causes the carriage motor to start the pickup moving outward to reduce the drive current of the actuator.

The TDRO terminal converts the tracking actuator drive current to voltage and the voltage is then amplified by IC7 and IC8. When the eccentricity of a disc is great, the actuator requires a larger drive current. This increase in the drive current of the actuator affects the carriage motor and causes it to turn, but since the carriage motor is slower to respond to a high frequency current this could damage the tracking servo operation. Because disc eccentricity increases the actuator drive current, the carriage servo control circuit gain must be kept low. The IC7(1/2) equalizer circuit performs this operation. The equalizer consists of C16, C17, C18, R75 and R76. The poles are 0.014Hz, 0.62Hz, and 136Hz.

When the carriage is shifted at high speeds such as during the scanning operation, the microcomputer T-O/$\overline{C}$ signal becomes "H." Q29, Q30 and Q31 also turn on and the IC7(1/2) gain is set to zero. As a result, the carriage servo loops open.

Next, the R-O/$\overline{C}$ signal becomes "L," and the $\overline{F}$/R signal selects the carriage movement direction. For example, when the $\overline{F}$/R signal is "L," Q26 and Q27 turn off, IC6 pin 5 becomes "L" and pin 13 becomes "H." This connects the analog switch between pins 1 and 2, and 12V is input to IC8(2/2) via R68 and R82. In this case, the R-O/$\overline{C}$ signal connects the analog switch between IC6 pins 10 and 11. A voltage of approximately 6 V is applied to the carriage motor.

During a jump operation, the carriage servo loop does not open, but the R-O/$\overline{C}$ signal and RA-G signal become "L," and the analog switch between IC6 pins 8 and 9 is connected. This sends the voltage divided by either R68 or R69 and R70 to IC8(2/2) and facilitates motor operation.

The operation of the carriage motor is controlled by the BTL circuit and is effected by a positive one-sided power supply. The amplified signals from IC7(1/2) with negative and positive cycles therefore, is changed by IC7(1/2) to signals with only positive cycles biared at 6V. IC5 generates the standard voltage for this purpose.

Carriage Control Circuit (SERVO UNIT CWX-560)

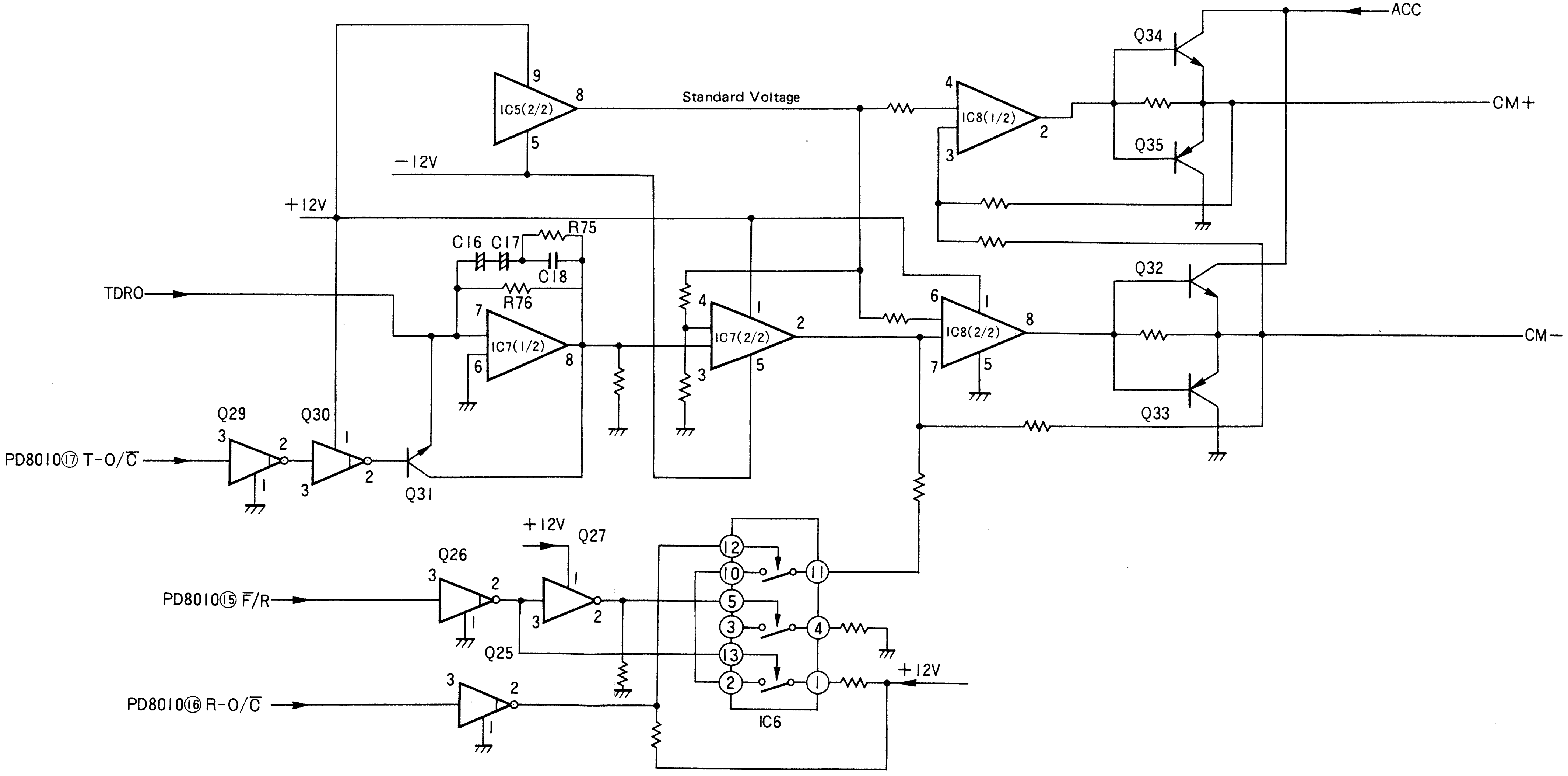


Fig. 10

3. EXPLANATION OF SIGNAL PROCESSING CIRCUIT FOR RF SIGNALS

3.1 RF EQUALIZER CIRCUIT (KHA301)

The RF signal is detected by the pickup and amplified at the RF amplifier of the main circuit board. In the process, the high frequency compoment decreases from the original spectrum. This is because, just as an electrical system has certain characteristics in relation to time frequencies, a light system also has certain characteristics in relation to spatial frequencies. This characteristic also has a constant delay period, and the RF equalizer circuit compensates for it. The compensation causes the "eye" pattern of the RF waveform to become wider in the direction of amplitude, and greatly improves the error rate after demodulation. The RF input from the main unit RF amplifier is input by IN+ (pin 1), and the RF-G input, by IN– (pin 2), so the equalizer output can be monitored from RFEQ (pin 12).

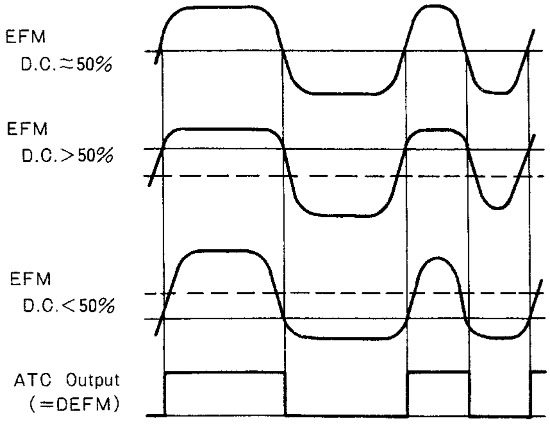


Fig. 11 ATC Circuit Operation

3.2 ATC CIRCUIT (KHA301)

The EFM signal loses its high and low range components when transmitted through the disc and pickup. Therefore it is necessary to recover the waveform it had during encoding before demodulation took place. That is, a sine wave-like waveform is converted to a square wave digital signal by designating those voltages higher than a given threshold value as "H," and those lower, as "L."

Since the pit shape is not consistent from disc to disc, the waveform of the EFM signal also varies. Therefore it is not possible to designate a constant voltage threshold. Furthermore, since the threshold voltage determines the switching timing from "H" to "L," and from "L" to "H," this value is important for the improvement of the error rate at the time of demodulation. For this purpose the ATC circuit utilizes the previously mentioned EFM signal characteristic to control the threshold value and convert the signal to a digital signal close to the the waveform that existed during encoding.

The output of the RF equalizer circuit is sent to the ATC circuit, converted to a digital signal by the ATC circuit, and output from pin 13 as DEFM signal.

It is conceivable that the noise that the ATC circuit generates when there is no input could have a bad effect on subsequent circuits. In order to prevent this, "H" output from pin 10 of IC9 (3/4) turns on Q1 when the F-T output is "L."

3.3 RF DETECTION CIRCUIT (KHA301

During the search operation, the microcomputer circuit designates the number of tracks to the target location by computing the data picked up from the TOC (which will be discussed later). As the carriage moves, it counts the tracks it crosses.

The laser beam may reach areas of the mirror surface in which there are no pits on the signal surface.

For this reason the RF detection circuit confirms that there are pits on the signal surface by detecting RF signals.

This output is designated as F-T and is sent to the microcomputer circuit from pin 25 of IC1 and is used as timing to detect mirror surface and to activate the focus servo circuit. The RF detection circuit also generates the HFD signal which carries the ON TRACK and OFF TRACK data necessary for track count and tracking during the search operation. This signal is sent to the microcomputer and the PLL IC from pin 24.

3.4 PLL CIRCUIT

Within the frequency spectrum of the EFM signal, there is a 4.3218 MHz component, which is the pit repeat frequency. The PLL circuit generates a continuous signal (PLCK) that is in synchronization with this signal.

Q2 and D8 make up an oscillating circuit (VCO) which controls frequencies with voltage input. The output of this circuit is sent to pin 9 of IC3 (TD6315P), reduced to 1/4 by the frequency division circuit, and then output as a PLCK signal from pin 12.

The EFM signal (DEFM) which undergoes waveform shaping by the ATC circuit is input from pin 14. The phases of the DEFM signal and the PLCK signal are compared inside IC3 each time the DEFM signal changes from "H" to "L," or from "L" to "H." The results of the comparison is detected by the difference of the pulse width of the two pulse signals output from pins 7 and 8. These two signals are added and input into a built-in operational amplifier.

The operational amplifier comprises a low-pass filter with C19 and R21 (from the feedback circuit); this output becomes the control voltage for the oscillation frequency of the VCO. In this way, using the DEFM signal transition timing as reference, the operational amplifier output voltage (at pin 4) is determined by the phase lead or lag (advance or delay) of the PLCK signal. For example, when the phasing is advanced, the oscillating frequency of the VCO is reduced by lowering the voltage. This keeps the phase difference at zero.

The PLCK signal is also used as a clock signal to generate the EFM1 signal. By using the PLCK signal as the clock for D-FF and the DEFM signal as input data within IC3, an EFM signal with a transition timing identical to the leading edge of the PLCK signal can be obtained. This signal (called the EFM1 signal) is output from pin 13.

The G terminal (pin 11) prevents operational error of the PLL circuit. When terminal G is "L," the two pulse signals for phase error data are not output and the impedance of pins 7 and 8 become high. Since C19 is not discharged, pin 4 maintains the same voltage as before, and the oscillating frequency of the VCO becomes constant.

This way, the PLL circuit prevents malfunctioning by maintaining the current state when:

- EFM signal is not input;
- The focus and tracking servo is not operating, or when
- There is a dropout in the EFM signal.

In addition, the TMO signal is sent to the PLL circuit from pin 48 of TC9178F, informing the PLCK signal frequency error.

The PLCK signal frequency is determined to be high or low by comparing its 11-cycle period with the maximum non-transition period of the DEFM signal. The result of comparison is output from TC9178F. The status of the TMO signal is described as follows:

When f(DEFM) > f(PLCK), "L" is output, and when f(DEFM) < f(PLCK), "H" is output. When f(DEFM) ≒ f(PLCK) or when output is inhibited, the impedance of output terminal (pin 48) becomes high. The criterion for this decision can be changed by the input of the TMWS signal (pin 43). When the TMWS signal is "L," the decision criterion is 11 ± 1 cycles for the PLCK signal, and when it is "H," it is 11 ± 0.5 cycles.

In order to improve the reliability of this decision, the TMO signal is output only after the same decision result is repeated a certain number of times; the number of such verifications can be switched by the input of the TMGS signal (pin 46). When the signal is "L," seven times; when "H," four times. In the actual circuit, both pins 43 and 46 are fixed at 5V.

The result determined in this way is effective as the TMO signal in expanding the capture range of the PLL circuit during normal reproduction. Since the DEFM signal is used as the decision standard, however, it may prevent the PLL circuit from locking in, which occurs in the process of disc motor starting up or recovering from an abnormal condition.

For this reason the output of the TMO signal can be controlled by external conditions. That is, when the $P/\overline{S}$ (Play/$\overline{\text{Stop}}$) signal (pin 21) is "L," the TMO signal is forced to be "H." When the $P/\overline{S}$ signal is "H" and the TMOE signal (pin 50) is "L," the output terminal (pin 48) of the TMO signal becomes high impedance. The FSPS signal (pin 51) (to be discussed later) is connected to pin 50.

3.5 TC9178F

IC4 (TC9178F) has been specially designed for the CD player to separate synchronous signals and to demodulate EFM signal. Its main functions are as follows:

1. Separation of synchronous signal,
2. EFM signal demodulation,
3. Subcode signal demodulation,
4. Demodulation of subcode signal P,
5. Demodulation of subcode signal Q,
6. Generation of CLV servo control signal, and
7. Generation of PLL frequency control signal.

These functions are explained below.

1.) Separation of Synchronous Signal

The encoded signal of the CD is 588T, which makes up one frame. (588T denotes the time span of 588 bits, or 588/(4.321×10^6)=136 μ sec.)

At the head of the frame, a synchronous signal called FS (Frame Sync) is attached. This signal becomes "H" for 11 clock cycles, and then "L" for 11 clock cycles. (In some cases, the low cycles come first.)

In the sychonous signal separation circuit, the FS pattern is detected by a logic circuit based on the EFMI signal from the PLL circuit. Depending on the quality of the EFMI signal, however, there is the possibility of erroneous detection; thorough checking is therefore performed.

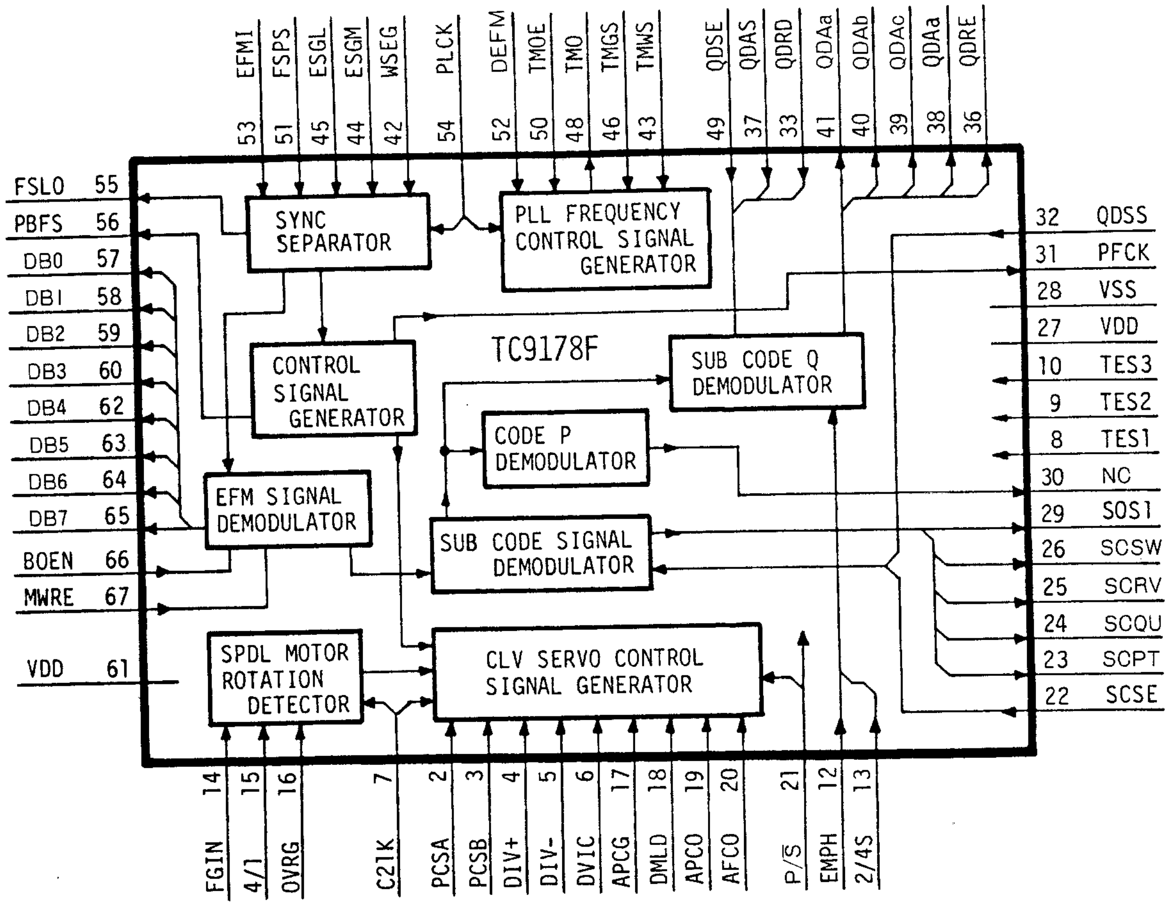

TC9178F
SYNC SEPARATOR
PLL FREQUENCY CONTROL SIGNAL GENERATOR
CONTROL SIGNAL GENERATOR
SUB CODE Q DEMODULATOR
CODE P DEMODULATOR
EFM SIGNAL DEMODULATOR
SUB CODE SIGNAL DEMODULATOR
SPDL MOTOR ROTATION DETECTOR
CLV SERVO CONTROL SIGNAL GENERATOR
53 EFMI
51 FSPS
45 ESGL
44 ESGM
42 WSEG
54 PLCK
52 DEFM
50 TMOE
48 TMO
46 TMGS
43 TMWS
49 QDSE
37 QDAS
33 QDRD
41 QDAa
40 QDAb
39 QDAc
38 QDAa
36 QDRE
FSLO 55
PBFS 56
DB0 57
DB1 58
DB2 59
DB3 60
DB4 62
DB5 63
DB6 64
DB7 65
BOEN 66
MWRE 67
VDD 61
32 QDSS
31 PFCK
28 VSS
27 VDD
10 TES3
9 TES2
8 TES1
30 NC
29 SOS1
26 SCSW
25 SCRV
24 SCQU
23 SCPT
22 SCSE
14 FGIN
15 4/1
16 OVRG
7 C21K
2 PCSA
3 PCSB
4 DIV+
5 DIV-
6 DVIC
17 APCG
18 DMLD
19 APCO
20 AFCO
21 P/S̄
12 EMPH
13 2/4S

Fig. 12 TC9178F Block Diagram

The PLCK signal generated in the PLL circuit is sent to a counter circuit that counts 588. The counter generates one window-detection signal for every 588 cycles of the PLCK signal. The window-detection signal has a specific time span designated by the WSEG signal (pin 42). That is, when the WSEG signal is "L," the time span is ±3 cycles from the finish time of the 588 count; when it is "H," the time span is ±7 cycles from the finish time. In the actual circuit, however, the WSEG signal is fixed at "L."

When the FS pattern is detected within this window detection range (range W), the circuit is reset by the timing at which it was detected, and the PLCK signal counter is reset. FS patterns can be separated at each 588T steadily by repeating the above operations. The FS pattern, aside from being used inside this IC, is output as the PBFS signal to pin 56.

When the PLL circuit is functioning properly, FS is equal to 588T, and is detected at the center of range W. The FS pattern is ignored when it is detected outside range W due to, for example, dropouts of EFM signal.

Even in cases where the FS pattern is not detected within range W, as soon as the counter circuit reaches 588, it is automatically reset. However, when the FS pattern is not detected for several frames in a row, the FSPS signal (pin 51) becomes "H," and is sent to OVRG signal (pin 16), indicating asynchronous condition. The number of asynchronous frames is determined by combining signals ESGM (pin 44) and ESGL (pin 45). In the actual circuit, pins 44 and 45 are fixed at 5V.

ESGL	ESGM	Frame number
L	L	12
H	L	8
L	H	4
H	H	2

Fig. 13 Switching using ESGL and ESGM signals

2.) EFM Signal Demodulation

As mentioned before, both the data signal and the error correction signal are contained in one frame of the encoded signal for a total of 32 symbols. The EFM demodulation circuit returns a 14-bit symbol to the original 8-bit NRZ signal.

Each of the 8-bit signals of the 32 symbols which have been demodulated are numbered U0 to U31. U0 to U11 and U16 to U27 are data signals, and U12 to U15 and U28 to U31 are error correction signals. The error correction signals are all reversed after demodulation.

The demodulated 8-bit signal is stored in the latch circuit. Thus, the MWRE signal (pin 67) changes to "L," having completed the preparation to send the data out. This signal is sent to pin 3 of IC6 (TC9179F). IC6 turns the BOEN signal to "L" to send out the data. IC4 (TC9178F) then receives this data at pin 66, and by turning the DATA BUS on, it sends the 8 bits from the latch circuit to DB0 through DB7 (pins 65, 64, 63, 62, 60, 59, 58, and 57). This data is sent to the RAM (HM6116ASP) of IC5 and written.

The PBFS signal (pin 56) is sent to IC6 (TC9179F) to indicate the frame borders.

3.) Subcode Signal Demodulation

The symbol following the synchronous signal (FS) of the encoded signal is a signal for control and display. The control and display signals for 98 consecutive frames are combined into one block. The 8 bits of control and display signals of the n'th frame (counted from the leading one) are called Pn and Qn through Wn (n=0-97).

The control and display signals for the leading frame and the next frame of that block (98 frames) are synchronous signals which indicate the beginning of a block. They are referred to as S0 and S1 respectively. In other words, P0 through W0 indicate S0, and P1 through W1 indicate S1.

The signals of 98 frames are joined from P to W, and are called channel P, channel Q and so forth. As a group, these are referred to as subcode signals. Among the subcode signals, the only ones used at present are channels P and Q.

Channel P contains block location information, which includes whether the block is in the middle of a selection, between two selections, lead-in or lead-out. Channel Q contains information such as the selection number, the time elapsed since the selection began, and the disc's catalogue number and copyright code. In the lead-in area, channel Q also contains the TOC (Table of Contents) which describes the contents of the disc. (Details of the TOC will be discussed later).

The subcode signal is divided and demodulated in synchronization with the PBFS signal, and is output as signals SCPT, SCQU, SCRV and SCSW (pins 23, 24, 25, and 26). The switching of the dual signal is performed by the SCSE signal (pin 22).

SCSE	SCPT	SCQU	SCRV	SCSW
L	P	Q	R	S
H	T	U	V	W

Fig. 14 Switching using SCSE Signals

When the subcode signal is S0 or S1, the SOS1 signal (pin 29) is set at "H." The PFCK signal (pin 31) is sent to the subcode output terminal as FS data, but the duty ratio of this signal is 50%. Therefore the subcode signal is switched in synchronization with the leading edge. Signals PFCK, SCQU, and SOS1 are read in as the subcode in the microcomputer circuit.

4.) Demodulation of Subcode Signal P

Aside from being output as the SCPT signal, the subcode signal of channel P, after being demodulated, is sent to the counter circuit to improve the reliability of the signal. Only after the same signal is sent five consecutive frams is the SCPD signal sent to pin 30. Nevertheless, when S0 or S1 is detected, when a frame is started after the FSPS signal has become "H," or when the input data pattern is determined to be in error, the counter circuit is reset and the SCPD signal is maintained at the previous value. The SCPD signal, however, is not used.

5.) Demodulation of Subcode Signal Q

The 98 bits composing channel Q for the subcode signal consist of the following:

- 0-1 (2 bits) Used for S0 and S1
- 2-5 (4 bits) Called "Control" Determines the presence of emphasis and becomes the flag for 2 channel/4 channel.
- 6-9 (4 bits) Called "ADR" Serves as the flag which indicates the contents of DATA-Q which follows.
  ADR=1 . . . normal mode (discussed later)
  ADR=2 . . . catalogue number of disc
  ADR=3 . . . copyright code, serial number, etc.
- 10-81 (72 bits) Called "DATA-Q," when the above-mentioned ADR is 1, the contents of the program area and lead-out area in 8 bit groups are as follows:

10-17 (TNO)	number of selections
18-25 (X)	selection index number
26-33 (MIN)	time elapsed in minutes after selection begins
34-41 (SEC)	time elapsed in seconds after selection begins
42-49 (FRAME)	number dividing one second into 75 parts
50-57 (ZERO)	all zero
58-65 (AMIN)	time elapsed in minutes from the starting point of the disc program area
66-73 (ASEC)	same time as above in seconds
74-81 (AFRAME)	number dividing one second into 75 parts

  In its lead entry DATA-Q has the data which indicates the contents of the disc program. This is called the TOC (Table of Contents). The 24 bits, 58 to 81, indicate the starting point of the selection. The selection number is indicated by bits 18 to 25. As soon as the disc is loaded, this TOC is read and stored in the register.

- 82-97 (16 bits) Called "CRC", this is the error correction signal in the data of channel Q.

The CONTROL of channel Q is output by 4-bit transmission, but it is also decoded in IC9178F and output to the system. That is, when a pre-emphasis is placed on a source signal, the EMPH signal (pin 12) becomes "H," and the de-emphasis circuit (Q3 to Q6) is activated. The 2 channel/4 channel flag is output as the 2/4S signal (pin 13), but it is not used in this unit.

The separation of the subcode signal is done in synchronization with S0 and S1 detection. Unless the EFM signals and the movement of the TC9178F circuit is accurately synchronized by the PLL circuit, however, reliable separation of the subcode is not possible.

For this reason the subcode signal Q demodulation circuit has functions for confirming the synchronization in order to facilitate the separation of the subcode signal. The criteria for determining synchronization can be switched by the QDSS signal (pin 32). When the QDSS signal is "H," the FSPS signal is "L." In addition to this, both S0 and S1 must be properly detected in order for the subcode signal to be read out.

When the QDSS signal is "L," either the conditions for the "H" state must be satisfied or the FSLO signal must be "L." In addition to this, S0 or S1 must be correctly detected in order for the subcode signal to be read. In this unit, however, the QDSS signal is fixed at "L."

6.) Disk rotation error detection

The EFM signal, which is picked up from the disc, is demodulated and written in sequence into the RAM of IC5. Processing such as error correction is done using the clock signal generated by an oscillator. Thus data must be read in accord with the internal clock.

To accurately control the rotation of the disc, rotation error is detected from the reproduced frame synchronization signal. This error information consists of frequency and phase.

The frequency error is expressed by how many clocks of certain frequency are detected within the four frames.

From TC9179F, a clock signal (2.1168 MHz) which serves as the standard is input to pin 7 as the C21K signal. This clock counts four cycles of the FS (4/7.35kHz=544 μ sec). When the frequency error is zero, this clock counts 1152 times.

The range of error detection is 1152 ± 128; anything within this range is output as a digital signal with a modulated pulse width. This is the AFCO signal (pin 20). When the error exceeds the detection range, the AFCO signal does not become a pulse signal, therefore the number of counts decreases. In other words, when the rotation of the disc is too fast, the AFCO signal is fixed at "L"; and transmitted when the count is excessive, it is fixed at "H" and transmitted.

When the error count exceeds 1152 ± 128 clock cycles, DMLD signal (pin 13) becomes "L," and when it falls below the range of 1152 ± 64 clock cycles, it becomes "H." Thus, the DMLD signal detects the frequency servo lock condition with some delay. The phase error of the frame synchronous signal is detected by comparing the signal with the standard clock signal for detecting phase errors which is used to count down the C21K signal.

Error detection is done for each N frames. The number N is designated by the combination of the PCSA and PCSB signals (pins 2 and 3). In this unit, N is 6 because the PCSA signal is set at "L" and the PCSB signal is set at "L."

PCSA	PCSB	N	Fc(Hz)
L	L	6	1225
H	L	8	918.75
L	H	12	612.5
H	H	16	459.375

Fc=7.35kHz/N

Fig. 15 Switching using PCSA and PCSB Signals

The detected phase error is output from pin 19 as a pulse-width-modulated signal, much like the AFCO signal for frequency errors. This is the APCO signal.

The amount of data being written into the RAM is constantly monitored by TC9179F. When this data reaches a certain amount and discrepancies form, TC9179F seeks the correction of the time axis with the signals of DIV+ and DIV–. These signals are input to TC9178F pins 4 and 5. By varying the countdown number which forms the standard signal from the C21K signal, the apparent phase error is adjusted. The variance in the countdown number can be designated by the DIVC signal (pin 6). In this unit it is fixed at "L," to be within ±1.

By setting the APCG signal (pin 17) at "L," phase error detection can be inhibited.

Accurate phase error detection is impossible when the frequency servo is not locked. For this reason, the DMLD signal, which determines whether or not the frequency is locked, is connected with the APCG signal.

When phase error detection is inhibited, the APCO signal designates the phase error to be zero. The duty ratio is fixed at 50%, and the standard signal is designated so that it matches the phase of the detected signal. Phase error is detected smoothly, starting at zero, and the servo operation takes place smoothly and stably.

The rotation control function by the FG signal is incorporated in the disc rotation error detection block. The FG pulse from the disc motor of the main unit is input to TC9178F FGIN (pin 14) and controls the APCO and AFCO output, so that the servo circuit keeps the disc rotation in the range of 175 to 740 rpm.

The number of FGIN pulses generated for each revolution of the disc motor can be designated by $\overline{4}/1$ (pin 15). When $\overline{4}/1$ is "H," one pulse; when "L," four pulses. In this unit $\overline{4}/1$ is fixed to "H." Thus, one pulse is sent for each revolution of the motor. The OVRG signal (pin 16) enables/disables the disc motor control by FGIN. Because FSPS is connected to OVRG in this unit, the motor control is enabled when FSPS is "H."

Disc motor rotation (rpm)	AFCO	APCO
– 175	"H"	Duty cycle fixed at 50%
175 – 740	Normal	Normal operation
740 –	"L"	Duty cycle fixed at 50%

Fig. 16

7.) PLL Frequency Control

As expalained under PLL circuit, this block generates the TMO sagnal.

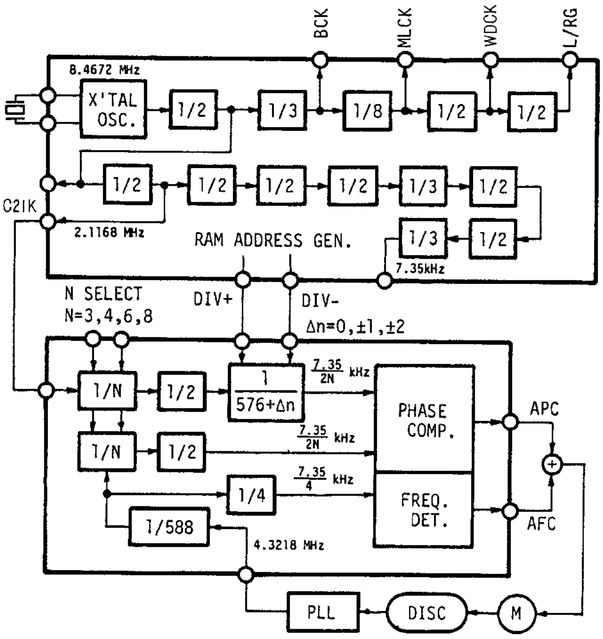


Fig. 17 Timing Signal and Frequency and Phase Control

3.6 TC9179F

IC6 (TC9179F) has been specially designed for the CD player to perform error detection and correction processing, as well as data jitter absorption.

For the theory and process involved in error detection and correction processing, refer to the product description of the PD-1. The main functions of the TC9179F are as follows:

1) Clock signal generation,
2) RAM control,
3) C1 and C2 error correction,
4) Data correction,
5) Digital attenuation,
6) Muting signal generation,
7) Data output, and
8) Data status output.

These block functions are described below:

1.) Clock Signal Generation

The clock signals required by TC9179F and TC9178F are generated by connecting a crystal oscillator to pins 52 and 53. The CKSE signal (pin 54) is input according to the frequency of the connected oscillator. The CKSE signal must be "H" in this unit to make the frequency 8.4672 MHz. The original oscillation frequency is frequency-divided to 1/4 and sent as the C21K signal (pin 56). The C21K signal is sent to TC9178F pin 7.

2.) RAM Control

Once the EFM signal has been demodulated, TC9178F uses the MWRE signal to inform the RAM that it is able to send data. Based on this, the TC9179F puts the RAM in the write mode with the CE1 signal (pin 17) and the R/W signal (pin 15). Then with the BOEN signal (pin 4), the TC9179F requests TC9178F to transmit data. The address location in which data is stored is controlled by the Ad- 0 to 10 signals (pins 5 to 14, and 18), which are generated using th PBFS sigal (pin 2) as a synchronization signal.

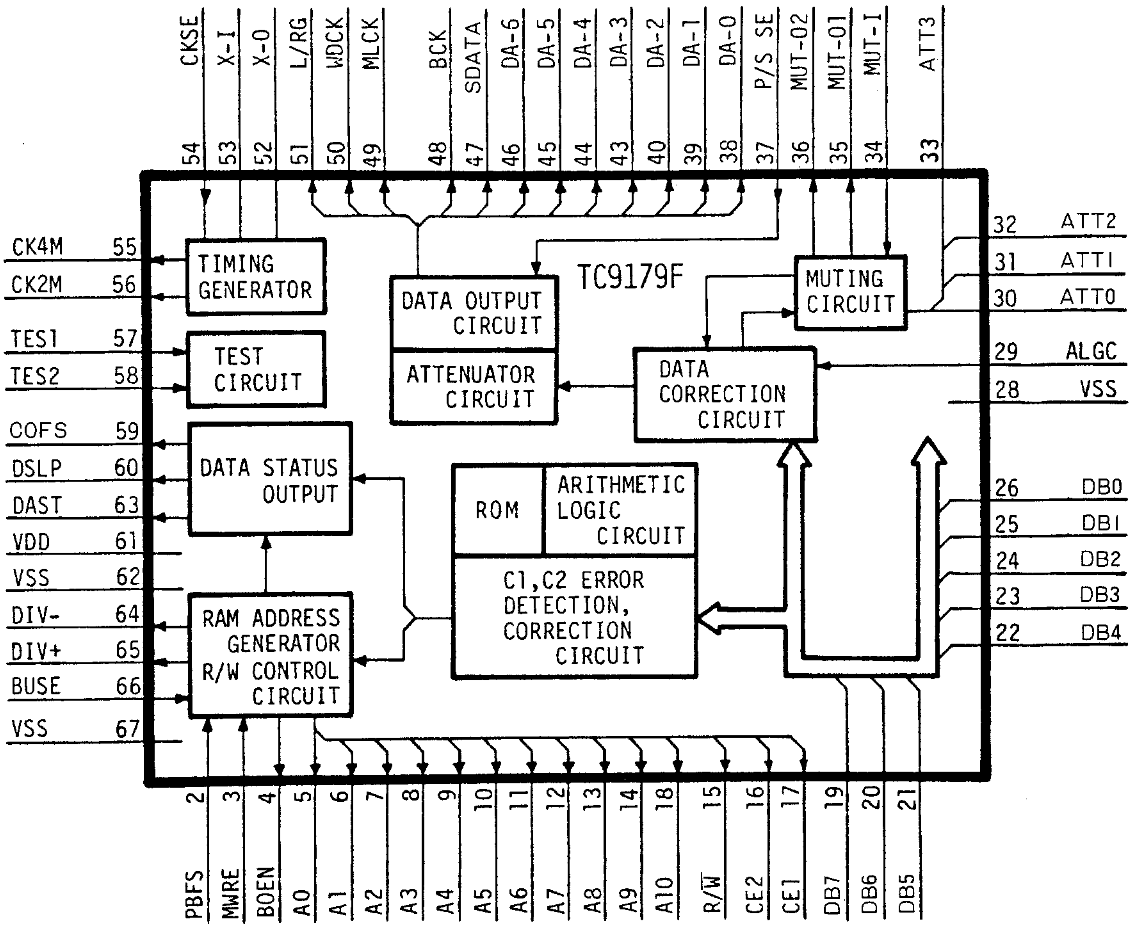

CKSE 54
X-I 53
X-0 52
L/RG 51
WDCK 50
MLCK 49
BCK 48
SDATA 47
DA-6 46
DA-5 45
DA-4 44
DA-3 43
DA-2 40
DA-1 39
DA-0 38
P/S SE 37
MUT-02 36
MUT-01 35
MUT-I 34
ATT3 33
32 ATT2
31 ATTI
30 ATT0
29 ALGC
28 VSS
26 DB0
25 DBI
24 DB2
23 DB3
22 DB4
CK4M 55
CK2M 56
TES1 57
TES2 58
COFS 59
DSLP 60
DAST 63
VDD 61
VSS 62
DIV- 64
DIV+ 65
BUSE 66
VSS 67
2 PBFS
3 MWRE
4 BOEN
5 A0
6 A1
7 A2
8 A3
9 A4
10 A5
11 A6
12 A7
13 A8
14 A9
18 A10
15 R/W
16 CE2
17 CE1
19 DB7
20 DB6
21 DB5
TC9179F
TIMING GENERATOR
TEST CIRCUIT
DATA STATUS OUTPUT
RAM ADDRESS GENERATOR R/W CONTROL CIRCUIT
DATA OUTPUT CIRCUIT
ATTENUATOR CIRCUIT
ROM
ARITHMETIC LOGIC CIRCUIT
C1,C2 ERROR DETECTION, CORRECTION CIRCUIT
DATA CORRECTION CIRCUIT
MUTING CIRCUIT

Fig. 18 Block Diagram of TC9179F

The amount of data stored in the RAM is constantly monitored. If the RAM capacity or its data processing ability is not sufficient, the disc motor servo is made to process this using the DIV+ and DIV– signals (pins 65 and 64). Normally these signals are both set to "L."

The criteria for excess or insufficiency can be changed by the BUSE signal (pin 66). In this unit BUSE is fixed at "H," designating ±2 frames. When the amount of data is insufficient by more than two frames, the DIV+ signal is set to "H." Conversely, when data is excessive by more than two frames, the DIV– signal is set to "L."

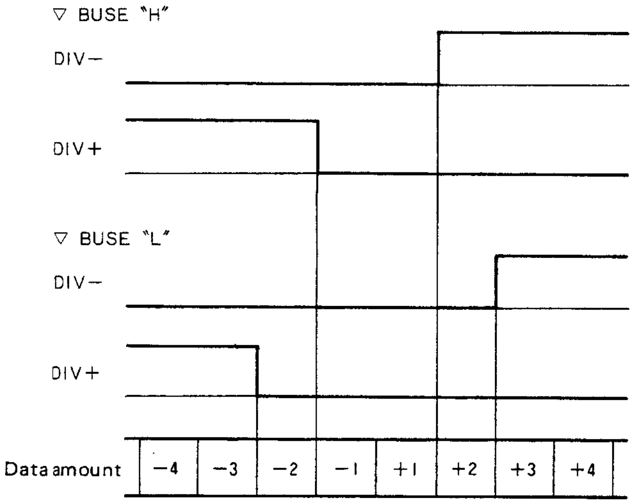


Fig. 19 DIV– and DIV+ signal

3.) C1 and C2 Error Correction

Error detection and correction in the CD player are done by two processes called C1 and C2. In order to prevent dropout of a group of data from sequential sampling data during the encoding process, the sequence is divided into three different steps. This process of division is called interleaving. At the time of decoding, the original data must be reassembled (de-interleaving) by an exactly reverse process.

As the first-stage de-interleaving, a one-frame delay is added between each symbol, and data is read out from the RAM. All odd numbered symbols are therefore moved back by one frame. With this method, the first frame to undergo C1 correction is reconstructed.

In the C1 correction process, correction is performed using the 28 through 31 error correction symbols (P parity) of the reconstructed frame. However, C1 only performs corrections when the number of errors per frame is 2 symbols or less out of 32. Correction is not performed when errors of three symbols or more are detected. In that case, all of the symbols (including those with no error) are set with a C1 error pointer. If the error is in two symbols, it is theoretically possible that the correction itself is done incorrectly, so the pointer is set after performing the correction process.

Thus an error pointer is set for all the symbols in a frame when more than two erroneous symbols are detected. Thus, the low reliability of data is detected by the C2 process. The P parity used in C1 is omitted here, and each frame is treated thereafter as consisting of 28 symbols. The symbols in which errors were detected and corrected are returned to the RAM and rewritten.

Next, for an n'th symbol, a 4xn frame portion delay is added for 28 symbols, and this is read out from the RAM. Thus, a zeroth symbol from a certain frame, and a first symbol from four frames preceding it and so forth. Thus, a 108 (4 x 27) frame portion is read out for the 27th symbols of the previous frame, to create one C2 corrected frame. (This is the second step of de-interleaving.)

In the C2 process, correction takes place using the 12th to 15th error correction symbols (Q parity) taken from frames reconstructed in the manner explained above. The C2 correction process can process up to three erroneous symbols for each set of 28 symbols.

C2 learns the C1 error detection results from the C1 error pointers on these symbols, compares them with its own error detection results, and performs the correction process only when the probability of erroneous correction is low. Symbol data with a low reliability is set in the C2 error pointer in the same manner as in C1; and the corrected symbols are rewritten in the RAM in place of the erroneous symbols. The error pointers of C2 are set while comparing them with the C1 error pointers.

Dn+1			Dn			Output data	
MSB –30dB	MSB C2EP	LSB C2EP	MSB –30dB	MSB C2EP	LSB C2EP	Processing	Processing result
X	0	0	X	0	0	Dn	Direct
X	X	X	0	0	1	Dn(MSB+80H)	Direct
X	0	0	X	1	X	(Dn – 1/2)+(Dn+1/2)	Average value
0	0	1	X	1	X	(Dn – 1/2)+(Dn+(MSB+80H)/2)	Average value
1	0	1	X	1	X	Dn – 1	Previous value
X	1	X	X	1	X	Dn – 1	Previous value
X	0	0	1	0	1	(Dn – 1/2)+(Dn+1/2)	Average value
0	0	1	1	0	1	(Dn – 1/2)+(Dn+1(MSB+80H)/2)	Average value
1	0	1	1	0	1	Dn – 1	Previous value
X	1	X	1	0	1	Dn – 1	Previous value

X: 1 or 0
Dn : Processed word data
Dn – 1 : Word data that has been output previously
Dn + 1 : Word data following the current one
MSB-30dB : "1" is set when the MSB data is below –30dB.
MSB C2EP : C2 error pointer of MSB data (Set to 1 when correction is not possible).
LSB C2EP : C2 error pointer of LSB data (Set to 1 when correction is not possible).
MSB + 80H : LSB is set at 80H (1000 0000).

Fig. 20 Data Correction Processing

4.) Data Correction

As shown in the specifications, the data that has undergone C2 correction then undergoes scramble and frame delay processing. (The third step of de-interleaving.)

This data is then sent one by one in the order of the words, starting from the LSB 8 bits. Simultaneously, the error pointers of C2 are checked, and a decision is made according to the reliability of the data whether to output directly, to correct it with the average value of the data before and after, or to output the previous data again. This decision is made by taking into account the C2 error pointers on the MSB and LSB data, and the level of the MSB data when it is being converted to an audio signal.

5.) Digital Attenuation

The level obtained by converting the output of TC9179F into an audio signal can be determined digitally by the AT-3 to AT-0 signals (pins 33 to 30). That is, the amount of attenuation is related to the four-bit digital values with AT-3 as MSB and AT-0 as LSB. Because this is negative logic, however, "1111" produces 0 dB, and "0000" produces – ∞dB.

In this unit, adjustment in a 6dB range is enabled by switching AT-2 with the hideaway switch.

ATT0	ATT1	ATT2	ATT3	(dB)
1	1	1	1	0
0	1	1	1	– 1.15
1	0	1	1	– 2.5
0	0	1	1	– 4.0
1	1	0	1	– 6.0
0	1	0	1	– 8.5
1	0	0	1	–10.1
0	0	0	1	–12.0
1	1	1	0	–14.5
0	1	1	0	–18.0
1	0	1	0	–24.0
0	0	1	0	–30.0
1	1	0	0	–36.1
0	1	0	0	–48.2
1	0	0	0	–60.4
0	0	0	0	–∞

Fig. 21 Amount of Attenuation by ATT 0 to 3 Signals

Pins 33 to 30 are I/O terminals; these pins serve as input terminals when the WDCK signal (pin 50) (88.2 kHz) is at one state, and the pins change their function to output terminals at the transition of the WDCK signal, thus changing their function at each WDCK transition. Therefore, the data in AT-3 to AT-0 is read when the WDCK signal is at "H," and the internal attenuate condition is output, when this is "L."

Sporadic data errors are corrected by the aforementioned data correction function, however, continuous erroneous signals must be corrected differently. When those of a short duration occur repeatedly, the frequency of this repetition becomes an audible component. When the error is of a long duration, problems like the output of a direct current arise. If such errors were detected and the output instantaneously halted, the signals would then lose their high quality sound. To solve this problem, a muting on/off function that operates smoothly without causing unnatural transitions (the fade-in/fade-out function) is incorporated.

The MUTE signal from the microcomputer circuit is connected to pin 34 and is input as the MUT-I signal. When the MUT-I signal is "L," the muting operation takes place every 16 frames and goes through seven gradual steps. Muting from 0 dB to – ∞ dB is performed in 1.36 msec. When the MUT-I signal is "H," the level returns gradually to 0 dB in the same manner.

6.) Muting Signal Generation

Aside from the muting command issued by the microcomputer circuit, TC9179F internally detects conditions where muting is necessary. When an uncorrectable error continues for a certain number of frames, or when the excess or insufficiency of the RAM data cannot be absorbed by the disc motor, the MUT-02 signal becomes "L." Or when the MUT-01 signal (pin 35) becomes "L," or when the de-interleaving is missed three times in a row, the MUT-02 signal becomes "L."

7.) Data Output

The data of the audio signal processed by the TC9179F can be output either in series or in parallel; the output method can be switched by the series/parallel signal (pin 37). In this unit the signal is set at "H" (serial transfer).

Data is transferred in sequence from the 16-bit MSB, and is output as SDATA signal (pin 47). Bits are transferred in synchronization with the BCK signal (pin 48): the next bit is transferred when BCK rises. The WDCK signal (pin 50) alternates its state at every eight bits or one symbol. A new word starts at the rise of the signal. The L/RG signal (pin 51) alternates its state at every word. "L" indicates the left channel signal, and "H" indicates the right channel signal.

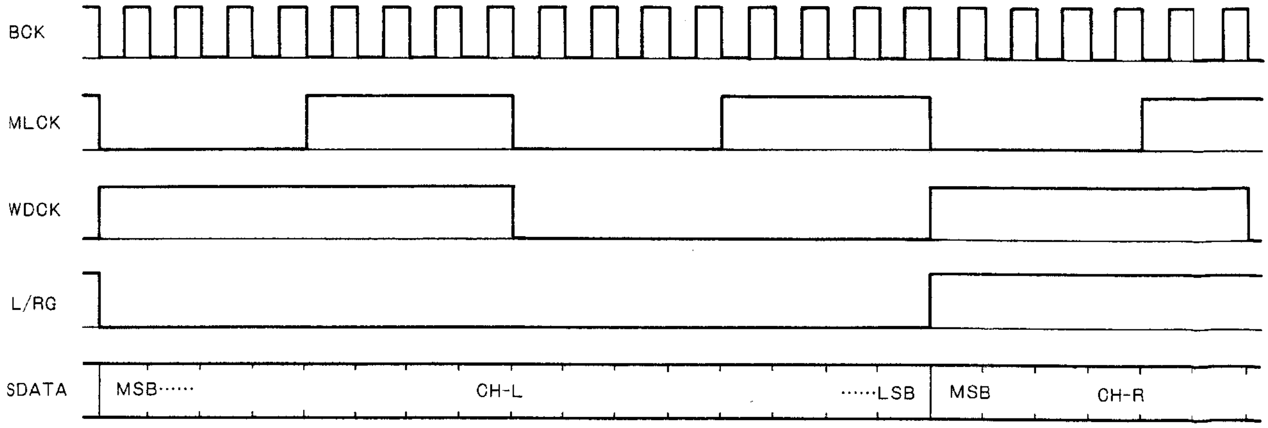


Fig. 22 Serial Data Output Timing Chart

8.) Data Status Output

A signal is provided to externally monitor the results of C1 and C2 correction error detection and the amount of data in the RAM. The signal is called the data status output.

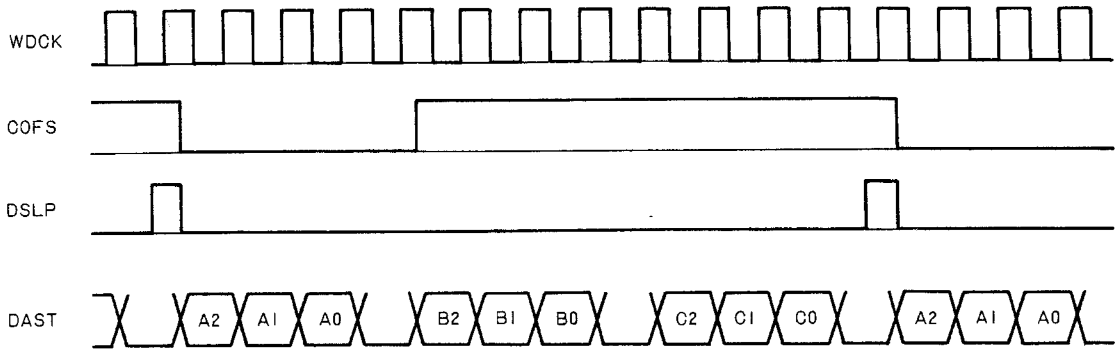


Fig. 23 Data Status Output Timing Chart

- A0, A1, A2 indicate the amount of data in the RAM

A0	A1	A2	Amount of Data (frame)
0	0	0	– 4
1	0	0	– 3
0	1	0	– 2
1	1	0	– 1
0	0	1	+ 1
1	0	1	+ 2
0	1	1	+ 3
1	1	1	+ 4

- B0, B1 and B2 indicate the correction error detection results

B0	B1	B2	Content	Correction	C1EP
0	0	0	No error	———	0
1	0	0	1 symbol in error	1 symbol	0
1	1	0	2 symbols in error	2 symbols	1
0	0	1	Unable to detect error	———	1

- C0, C1, C2 indicate the C2 correction error detection results

C0	C1	C2	Content	Correction	C2EP
0	0	0	No error	———	0
1	0	0	1 symbol in error	1 symbol	0
0	1	0	2 symbols in error	2 symbols	0
1	1	0	3 symbols in error	3 symbols	0
0	0	1	Unable to correct data	———	I
1	0	1	Unable to correct frame	———	A

Fig. 24 Contents of Data Status Signal

3.7 DISC DRIVE

When the P/S signal (pin 21) becomes "H," the frequency error detection circuit begins to function. Since the rotation is still slow, fixing the AFCO signal at "H," and the frequency servo is not locked, the APCO signal is fixed at 50% duty ratio.

Since the RF signal is not given, the HFD signal from the RF detection circuit is "L," so the PLL is in a hold state. During this time the AFCO signal is "H." When the RF signal that is accelerated at the maximum capacity is input to the disc motor, the HFD signal starts alternating between "H" and "L." The PLL then begins to function, making the TMO signal effective, and thereby increasing the oscillation frequency of the VCO.

By the time FS patterns are detected, the FSPS signal becomes "L," and the TPO signal is cancelled.

When the PBFS signal is determined to be frequency locked, the DMLD signal becomes "H," and the phase servo begins to function and reaches a stable condition.

Since AFCO and APCO are pulse modulated signals, they are converted to level information by the LPF.

When the stop condition is reached, the P/S signal of IC4 becomes "L," the AFCO signal becomes fixed at "L," and the disc motor decelerates and comes to a stop.

P/S	OVRG	AFCO	APCO
L	L or H	L	D.C.=50%
H	L	Normal operation	

Fig. 25 Frequency and Phase Servo Cancel

3.8 AUDIO CIRCUIT

16-bit serial data is sent from the signal processing LSI (TC9179F) to the TD6705AP D/A converter after being synchronized with the trailing edge of the BCK shift clock. This data is read from the leading and trailing edges of the TC9179F L/RG output. When the L/RG is "H," R channel data is taken in and when it is "L," L channel data is taken in. The following example (L channel sound reproduction) assumes that the L/RG signal is "L."

The 16-bit data taken into the TD6705AP L channel register is divided into 9 bits for the MSB side and 7 bits for the LSB side. They are each stored in counters, which then begin counting down. The two power sources for MSB and LSB that were derived from the IREF pin (current ratio = 128:1) begin to charge C60 (which is connected to L1 and L0) when the countdown begins. When the count reaches zero, the constant power supply is cut off and the D/A conversion is complete.

As a result of the D/A conversion, DC voltage appears at the internal integrator output (LO). The built-in deglitcher circuit is activated by the TC9179F MLCK timing. It is converted to a 44.1 kHz, Duty Cycle 50%, PAM wave to be output to the LOUT. C60 is simultaneously discharged by the TD6705AP discharge to prepare for the next D/A conversion.

The above operations are synchronized with the L/RG. That is, L and R are alternately repeated in 44.1 kHz cycles and PAM waves are output to LOUT and ROUT.

The sampling frequency components of the PAM wave include the upper and lower side band components and higher harmonic wave components. Therefore, the PAM wave is passed through buffer amplifier IC13, and then the noise component is eliminated at CWW-225 LPF.

The IC16 amplifier includes a de-emphasis circuit. When there is emphasis due to the EMPA signal sent from TC9178F, Q3 turns Q4 on, which then turns Q5 and Q6 on to perform de-emphasis. After that, the signal goes through the IC17 isolator circuit and a maximum audio signal of 281 mV is output to L and R.

Q7 and Q8 are muting circuits. They eliminate the popping sound that occurs when turning on the power.

4. THE CD PLAYER CONTROL SYSTEM

The PD3023A system controller has absolute control of the CDX-1 unit.

The system controller (PD3023A) in the servo unit controls the key display controller (PD6029) and the random access controller (PD8010) functions. The key display controller controls the FL display through the display drive IC (PD7005).

The main functions of PD6029 are to read key data from the 4x3 key matrix, and to control the display through PD7005. In addition to these, it also controls or monitors the following conditions of the mechanism:

● High temperature sensing terminal	TEMP
● KEY touch BEEP control	BEEP
● Pickup home position detection	HOME
● LD ON/OFF control	LD
● Loading mechanism control system	
● LOAD command output	LOAD
● EJECT command output	EJ
● Front switch detection	FRONT
● INTER LOCK detection	INTER LOCK
● Disc presence detection	DISC

These functional commands are input and output through PD6029. Since the PD6029 has no intelligence of it own, however, it cannot independently detect the status of a particular sense port and then activate another control port. It only outputs control signals according to PD3023A commands. The loading function operates as follows:

1. PD3023A regularly sends command to PD6029 regarding the status of the loading mechanism.
2. Each time PD6029 receives such a command, it sends the FRONT, DISC and INTER LOCK status back to PD3023A.
3. Based on the data sent back from PD6029, PD3023A determines the status of the loading mechanism and sends PD6029 the command for output to its LOAD or EJ pin.
4. PD6029 then activates either LOAD or EJ according to the command.
5. The LOAD or EJ command sent by PD6029 turns the loading motor with the loading motor driver, and moves the disc tray.
6. As the status of FRONT, INTER LOCK and DISC change with the movement of the disc tray, PD3023A detects these changes, and sends motor control commands to PD6029 according to the conditions at the time. PD6029 then starts LOAD or EJ operation in accordance with the given command.

As seen above, PD3023A controls all of the functions, even when PD6029 is started by PD3023A. After PD3023A is reset and started, the ENAB terminal becomes "H" to send a supply voltage of 5V (switched 5V) to PD6029. PD6029 uses this power to start its own POWER ON reset circuit.

The primary purpose of the random access controller (PD8010) is to control the servo system (e.g., focus servo, tracking servo); it has the following input and output terminals:

Focus servo system – PUSH, LOOP, FT
Tracking servo system – J–, J+, T-AS, HFD, DTE
Carriage servo system – T-O/C, R-O/C, F/R

Also as an interface with PD3023A, it has data lines DO0 to DO3, Sel0 and Sel1 (which select the data setting area within PD8010), LOAD for data strobe, and INT signal output for signals from PD8010 to PD3023A.

E is the PD3023A clock division output (1 MHz) and is used as the clock for PD8010.

In addition to controlling the whole system through PD6029 and PD8010, the PD3023A circuit functions as a system controller to control the system reset start check with the reset circuit. It also checks the back-up memory, interface with externally connected circuits such as a CENTRATE unit through the AUX control circuit, and the DC-DC converter (main power source) ON/OFF. Functions that the PD3023A performs directly are: reading the subcode with the S0S1, SCQU and PFCK lines; starting and stopping the spindle motor with P/S; muting the audio circuit with MUT; controlling the carriage servo with ON/OFF and RA-G; switching the tracking servo frequency range with T-N/W; and detecting temperature increases inside the hideaway with TEMP.

● Temperature Sensor Function

The temperature sensor signals are TEMP sent to PD6029 of the player, and TEMP sent to PD3023A. The sensors are placed separately in the player section and the hideaway unit to monitor rises in temperature inside that unit. If either one detects an "L," the POWER, and AUX B signals of PD3023A become "H" to control the temperature increase, and the main power supplied to the servo system is turned off. Operations are stopped until the temperature drops and both TEMP signals (PD6029 and PD3023A) become "H." When this function turns off the power the display shows "HH HHHH" to indicate that it is in a non-operating condition. It is still possible to perform the loading and eject functions in this non-operating condition.

• Key display

— Key Scan —

Negative pulses are sent in order (from KS0 to KS3) by PD6029 pins 28 to 32 according to the timing shown in Fig. 26. This pulse is output constantly while Vcc is being applied to PD6029.

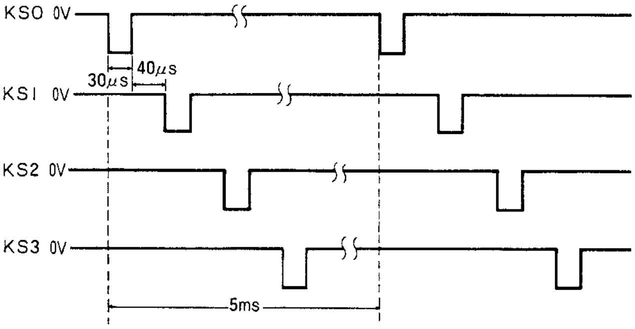


Fig. 26 KEY SCAN Timing

Each of the PD6029 pins (KS0 to KS3) reads the KD0 – KD3 data when it becomes "L."

When no keys have been pushed, KD0 to KD3 are all "H." Since there are only eight keys on the keyboard in this unit, and they are composed of a 4x3 matrix, KD0 is not used, and it is connected to +5V.

— Display —

48-bit (4 bits x 12) display data is sent through the 4-bit bidirectional interface from the system controller (PD3023A). After converting this data at PD6029 to bit image data (segment data and grid data) (80 bits) which is compatible with PD7005, PD6029, CS (pin 34) is set to "L" to notify PD7005 that data is about to be transmitted. From SDATA (pin 24) the data is transmitted serially in 80-bit segments synchronized with the SCK leading edge. After this, CS (pin 34) is returned to "H" and the transmission is ended. It takes an average of 1.5 msec to send this data to PD7005. The DRST is another line which connects PD6029 and PD7005. It is used to clear data sent to the PD7005 (entire display is erased) when the unit is being used in the set up or search mode, and the display is blinking. In this condition, the DRST changes from "H" to "L" in synchronization with the blinking display. During normal steady display, the DRST is "L."

PD7005, which receives the display data from PD6029, performs the internal register rewrite and outputs signals in synchronization with the grid output of eight pins (pins 12 to 15 and 40 to 43), and with the segment output of ten pins (pins 18 to 22 and pins 34 to 38). PD7005 pin 26 has an applied voltage of –30 V, and pins 18 to 21 and 34 to 37 are connected to –30 V with resistors. This results in an output which varies between –30 V and 5 V. When the grid and segment are "H," the FL lights up, but the FL filament will not light unless a 3 Vrms alternating current biased to –22 V has been applied.

5. MICROCOMPUTER SYSTEM OPERATIONS

5.1 INITIALIZING FUNCTION

The Schmitt trigger composed of Q1 and Q2 detects voltage applied to ACC. Through D2, the pulse generator composed of Q3 becomes "H." As a result, an "L" pulse (approximately 30 ms) to pin 6 in the system controller (PD3023A), and the reset cycle is started.

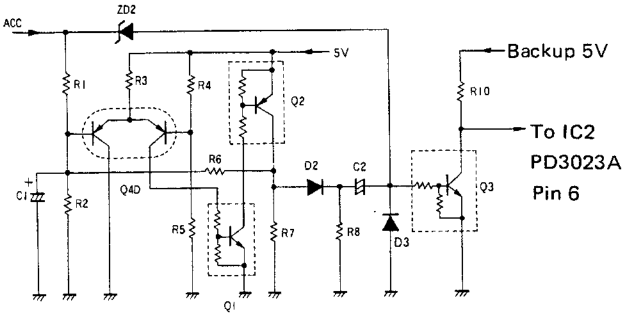


Fig. 27

Since the Q3 collector is connected to the backup power supply (5 V) by R10, PD3023A pin 6 remains at "L" unless the product is also connected to the power supply. This unit was constructed so that the reset cycle does not start unless the product is connected to the backup power spply. (See Fig. 27.)

When PD3023A is reset and started, along with initializing all circuit ports, data is written into PD8010 through data BUS DO0 to DO3 to perform initialization. Then, to start the KEY and DISPLAY controller (PD6029), PD3023A pin 11 is set to "H" to turn Q13 and Q12 on and supply switched 5 V. At this point, all initial processing is complete and a four-second non-operating period begins.

5.2 STARTING FUNCTION

After the four-second non-operating period, the system controller (PD3023A) begins transmission to the KEY and DISPLAY controllers (PD6029) through the 4-bit bi-directional interface. These begin to exchange the following:

- the status of the loading mechanism
- the status of the keyboard
- display data

(The negative pulse sequence with a pulse width of approximately 120 μs is regularly recorded by collectors Q14 to Q18.)

When the pickup is not in the home position (when PD6029 pin 9 is "H"), $\overline{\text{RA-G}}$ PD3023A (pin 23) and PD8010 F/R (pin 15) are both set to "H," and a pulse (as shown in Fig.28) is sent from PD8010 R-O/C (pin 16) until the pickup comes to the home position.

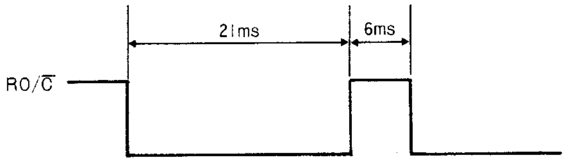


Fig. 28 Home Position Movement Pulse

While the above operation is taking place, the loading mechanism is checked. When the disc is not securely in place in the mechanism (when the PD6029 $\overline{\text{INTERLOCK}}$ (pin 6) is "H"), the PD6029 EJ output (pin 2) is set to "H." Then, S10 turns the loading motor making it EJECT until PD6029 $\overline{\text{FRONT}}$ (pin 5) sends an "L" signal.

After the above operation is finished, the DISB voltage is checked. When DISB is 0 V, PD3023A pin 18 is set to "L," and Q8 and Q151 are turned off. This starts the DC-DC converter (the primary power supply for the servo and signal processing circuits), which readies the unit for the PLAY operation.

5.3 AUX CONTROL CIRCUIT

Since the AUX circuit connects with a CENTRATE NEW LONSOME or some other system, it relays such commands input from the AUX connector to the system controller (PD3023A). The AUX connector, as shown in Fig.29, consists of six lines: AUX+B, ILL, DIS B, L, R, and G. The AUX circuit also supplies AUX+B to the outside.

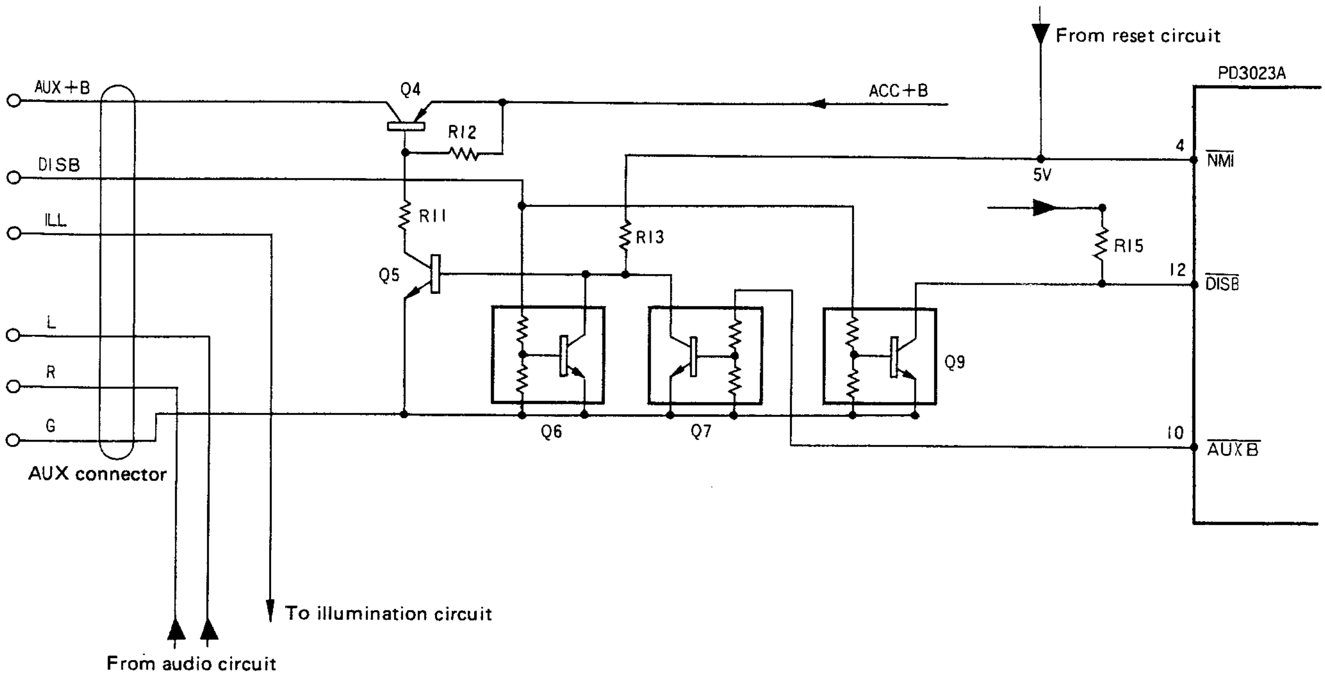


Fig. 29 AUX Control Circuit

The DIS B line is the external control input line, and when voltage (12 V) is applied, Q9 is turned on, PD3023A DISB (pin 12) becomes "L," and all operations are halted. It then goes into a non-operating period until Q9 turns off again and pin 12 becomes "H." Q6 turns on at the same time. As a result Q5 and Q4 both turn off, and the AUX+B output also stops.

This AUX+B output indicates to external circuits that this player is in operation. Normally when the player is operating, both Q5 and Q4 are on and ACC+B is output. If, however, a stop operation command comes from the outside, or a disc is ejected and the player stops by itself, "H" is sent from PD3023A pin 10, Q7 is turned on, and Q5 and Q4 are turned off to stop the output of the AUX+B signal.

The pullup resistance (R13) of the Q6 and Q7 collectors are connected to the reset circuit. This is to instantly stop the AUX+B output when the ACC power source ceases, and has no relation to the original circuit operation.

The ILL line is for night illumination; it is activated in synchronization with other apparatus. In this unit the line is directly connected to the illumination circuit.

L and R are audio outputs with a maximum signal amplitude of 281 mV.

5.4 LOAD AND EJECT OPERATIONS

The load and eject operations are started by the EJECT/RELOAD button as well as the internal DISC detection switch (S12).

The mechanism consists of three switches and a loading motor (LM) for moving the disc tray. The three switches are:

1. the FRONT switch (S10) which detects that the disc tray is set inside and the unit is in the play mode,
2. the INTER LOCK switch (S11), and
3. the detection switch (S12)

The loading operation begins when a disc is inserted into the empty slot and reaches the designated position so that the DISC detection switch (S12) turns off, causing PD6029 pin 4 to change from "L" to "H." When this change is detected, the PD6029 terminal LOAD (pin 3) becomes "H" and the loading motor driver (IC7) turns the loading motor to take in the disc. When the INTER LOCK switch (S11) is closed, PF6029 pin 6 becomes "L," pin 3 is returned to "L," and the loading operation is completed. At this time the display "DISC SET" is lit up and the completion of loading is indicated. The unit goes on to the set up mode (discussed previously under Starting Function). In this mode, the DISB check and play preparatory operations take place.

When the disc is already in the tray, (that is, when the disc is to be reloaded after having been ejected and not removed), just pressing the EJECT/RELOAD button makes PD6029 pin 4 change from "L" to "H," starting the loading operation.

The loading operation protective functions become activated in the following situations:

- When the disc is removed during loading and PD6029 pin 4 becomes "L."
- When the EJECT/RELOAD button is pressed during loading.
- When the INTER LOCK switch does not close within 6 seconds after loading is begun.

In these situations, the protective circuits halt the loading operation and PD6029 pin 3 becomes "L" while pin 2 becomes "H." This reverses the loading motor and ejects the disc.

If the INTER LOCK switch (S11) is closed, the eject operation is performed under the following conditions:

- The EJECT/RELOAD button has been pressed.
- The focus servo circuit cannot be activated within 5 seconds after the focus servo circuit activation command is given.

PD6029 outputs "H" to EJ (pin 2) and turns the loading motor in the eject direction. When the disc tray is sent out, the FRONT switch closes, and PD6029 pin 5 becomes "L," then PD6029 returns pin 2 to "L" and completes the eject operation.

In cases where the eject operation is not completed within 6 seconds after starting, the system controller (PD3023A) takes the unit back to the condition before reset was begun and terminates the operation. To get out of this condition either:

- push the clear button, or
- turn the power off and on.

This will reset the system controller (PD3023A).

When the EJECT/RELOAD button is pressed during normal operation (Play, FF, Search, etc.) the eject function takes precedence over all other functions. The servo operation stops, and at the same time the pickup moves to home position.

5.5 SETUP MODE

When the above starting function is completed, the main power source begins the setup mode. This setup mode is a preparatory operation performed before proceeding to the play operation. The following operations are performed in succession to put the circuits in the servo system in operation:

- Start the spindle motor
- Light the LD
- Start and confirm the focus servo circuit activation
- Activate the tracking servo circuit
- Read the TOC (Table of Contents)

Since only the "DISC SET" display flashes on and off during the setup mode, it is easy to verify the operation of this mode by looking at the display. Each operation in this mode is explained below:

• Start the Spindle Motor and Illuminate the LD

In the starting function, PD3023A pin 18 is set at "L." Approximately 100 msec after the main power source is activated this operation begins, and P/$\overline{\text{S}}$ (pin 20) is turned to "H" and the spindle motor is started. At the same time AUX B (pin 10) is turned to "L" and AUX B is sent to indicate an operating condition to the external CENTRATE unit. In addition, a command is sent to PD6029 to turn $\overline{\text{LD}}$ (pin 1) to "L," causing the LD to light up. The LD output of PD6029 is connected to the LD illumination control of the APC circuit, by an OR connection through D10-1 and D10-2 of $\overline{\text{INTER LOCK}}$ (pin 6). In other words, it is designed so that unless the $\overline{\text{LD}}$ output and the INTER LOCK are "L," the LD is not illuminated. This is to reduce the possibility of the LD being lit inadvertently by PD6029, erroneously sending an "L" to pin 1.

• Activating the Focus Servo Circuit

378 msec after the spindle motor starts (when the revolutions of the spindle motor and the illumination output of the LD reach their designated values) the system controller sets PD8010 (pin 13) to "L" and a command to move the lens is sent to the focus servo circuit. When the lens reaches the focal point and pin 9 becomes "H," the leading edge turns the PD8010 PUSH and LOOP to "H," and activates the focus servo by closing its servo loop.

During this time PD3023A monitors the focus servo circuit activation in 27 msec intervals with FT, and confirms that the focus servo circuit activation has been completed when "H" is detected four times in a row. If the focus servo circuit is not activated within five seconds, the operation is stopped, and the eject operation begins.

• Activating the Tracking Servo Circuit

When the focus servo circuit is successfully activated, it becomes possible to read out RF signals from the disc. By extracting the clock component from the RF signal, the spindle motor servo begins to function so that the spindle motor servo switches to the quartz servo. A waiting period of 432 msec is provided as a time margin for the activation of the quartz servo. Then, PD8010 T-O/$\overline{\text{C}}$ is turned to "L" and PD3023A T-$\overline{\text{N}}$/W is turned to "H" in order to send the tracking servo circuit activation command. After this an 80 msec time margin is provided for the servo circuit activation. Finally, PD3023A T-$\overline{\text{N}}$/W is returned to "L."

Since the data recorded on the disc can be read accurately after the tracking servo circuit is activated, PD3023A begins reading the subcodes from the signals which are sent to three terminals: PFCK (pin 39), SCQU (pin 31), and S0S1 (pin 30). Using the CRC code within the subcode, the system controller confirms to determine whether or not the signals are being read accurately. When the subcode has been read a maximum of 37 times (approximately 1 sec) and still no accurate data has been obtained (just as in problems during focus servo circuit activation) the disc is ejected. This function makes it possible to detect when a disc has been loaded upside down.

• Reading the TOC

When both the focus and tracking servo circuits are successfully activated and the signal can be read, the pickup is positioned within the program area. The setup mode will begin after the pickup moves to the home position.

From this program area, the absolute address of the subcode is read. Then the recorded distance to the TOC area (lead-in area) is computed, and finally the pickup is moved exactly that distance to begin reading the TOC.

The contents of the TOC are organized and stored in the RAM of PD3023A. When the number of selections recorded in the disc is 24 or less, as soon as the data for all selections is read, it starts searching for the beginning of the first selection.

The TOC is not always read at the end of the setup mode. This is done only when it is necessary to read the contents of the TOC (i.e., when a new disc is loaded into the unit). If PLAY is interrupted during normal operation by DIS B input, it is possible to move directly and resume playing at the pickup location before the DIS B input (The last address memory function recalls the absolute address).

5.6 SEARCH MODE

In response to a given situation, a search operation is performed in three steps: cross count search, step search, and cueing.

• Cross Count Search

This operation computes the direction of movement and the number of tracks from the current address to the target address. The direction of movement is set by F/R (pin 15) of PD8010. At the same time, TO/C̄ (pin 17) is set to "H," and R-O/C̄ (pin 16) to "L." Then the established voltage is applied to the carriage driver to move the pickup. A two-phase cross pulse goes to HFD (pin 10) and DTE PD8010 (pin 12) respectively each time a track is crossed. The direction of the track crossing is recognized by the phase difference. The number of tracks crossed increases with each pulse. When the pickup is moved in the desired direction, the number of tracks in the register decreases. When it moves in the opposite direction, the number increases so that the pickup only moves the exact number of tracks just computed.

If a disc is off center while the pickup is being moved, the pickup speed in the radial direction of the disc becomes negative. This means that even though the pickup is supposed to be moving toward the outer edge of the disc, it actually moves toward the inner edge. This is done to make it possible to move the exact number of tracks calculated.

When the designated number of tracks is crossed, F/R (pin 15) gives an output opposite to the previous one in order to stop the pickup. At the same time TO/C (pin 17) is turned to "L." In order to keep the "braking" time as small as possible within a range of 2 to 15 msec, the value computed during the initial calculation, for the number of tracks to be moved, is used to determine the stopping time.

When the "braking" period is over, the system controller returns R-O/C PD8010 (pin 16) to "H," and the move command for the pickup is ended. After the tracking servo circuit activation time (waiting period of 80 msec), just as during the setup mode, the current address is read again.

Then the track number difference from the new address to the target address is again computed. When the number of tracks to the target address is above 30, the cross count search is performed again. When the number of tracks to the target address is below 30, the pickup performs multi-jumps for that number of tracks in order to jump right to the target address and then go on to the next cueing step.

The above cross count search can only be conducted when the target address is known. This search type can be used only when the TOC data is usable, and when searching for the last address memory location. In all other cases, the step search explained below is performed.

• Step Search

The basic functions of moving the pickup and the braking output is the same as in the above-mentioned cross count search. The step search is performed when the target address is not known. Since the number of tracks to the target cannot be computed, a certain value is designated and the target address is approached in several steps.

First, the number of tracks to be moved is designated as 1280, and the pickup is moved this number. The address that the pickup reaches is checked, and the pickup is moved repeatedly in increments of 1280 tracks until the target is passed. When the target address has been passed, the movement of the pickup is reduced to 1/2 and the movement direction is reversed. Each successive time the target is passed, the amount of movement in the pickup is halved and the direction is reversed. The pickup movement is repeated in this manner until either the target address is hit, or the movement of the pickup is less than 20 tracks. After this it proceeds to the cueing step.

• Cueing Step

In the processes of cross count search and step search, the quartz servo of the spindle motor may be disturbed when the pickup moves quickly in the radial direction of the disc. It is necessary to remove the activation margin of the quartz servo and to decide the timing for the muting release. For this reason, it is necessary to stop the search operation three frames ahead of the original target address and switch to the play mode.

Although the accuracy of the direction of pickup movement is increased in the cross count search, there is a need to perform a final fine adjustment of the pickup position before proceeding to the play mode. This is because the reliability of the data originally recorded in the TOC is only accurate to one second. Because of this, the cueing step combines single track jumps and multi-track jumps to move the pickup to the designated address.

The jumping movement utilizes the PD8010 jump control logic section. The direction of the jump is set in PD8010 F/R (pin 15), turning T-AS (pin 18) to "H." Next, either J̄– (pin 20) or J̄+ (pin 19) sends out a 190 μs "L" pulse. Which signal is issued depends on whether the pickup lens is moved toward the center or toward the outside edge of the disc. After this, the pin (19 or 20) that did not send the signal to move the lens sends out a 210 μs "L" pulse to stop the pickup movement. While the above pulses are being sent, T-AS (pin 18) detects the change in polarity of the signal sent to DTE (pin 12) and returns to "L." This completes the jump operation, but a 3 msec waiting period is provided to allow the servo to stabilize.

The above process is the sequence for one jump. During this operation, T-W/N̄ is set at "H" to expand the tracking servo span. Multi-jumps are performed by repeating the jump sequence described above.

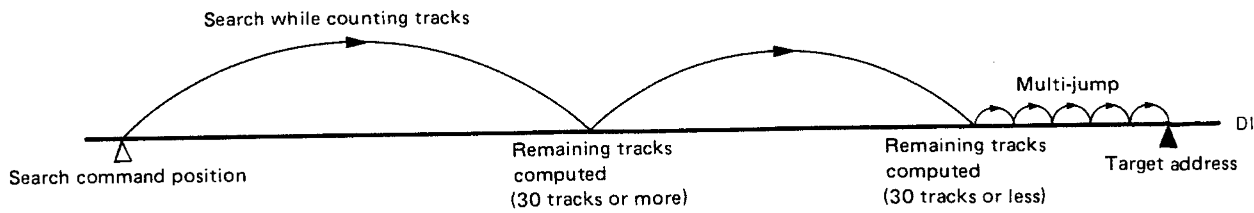

Search while counting tracks
Multi-jump
DISC
Search command position
Remaining tracks computed (30 tracks or more)
Remaining tracks computed (30 tracks or less)
Target address

Fig. 30 Cross Count Search (When the target address is known)

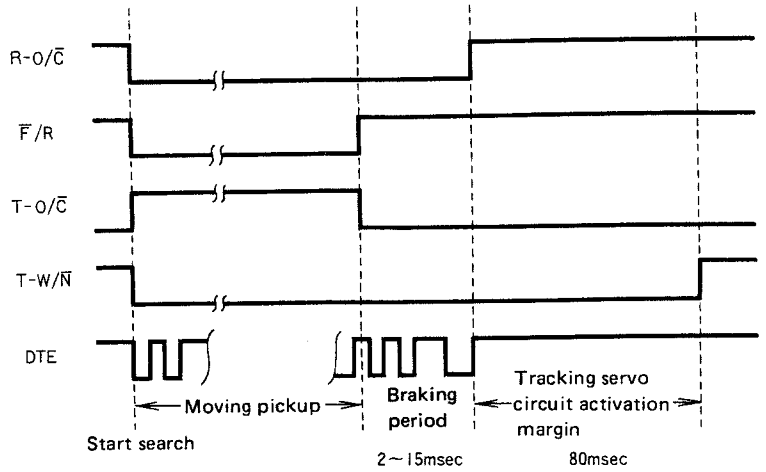


Fig. 31 Timing Chart of Search

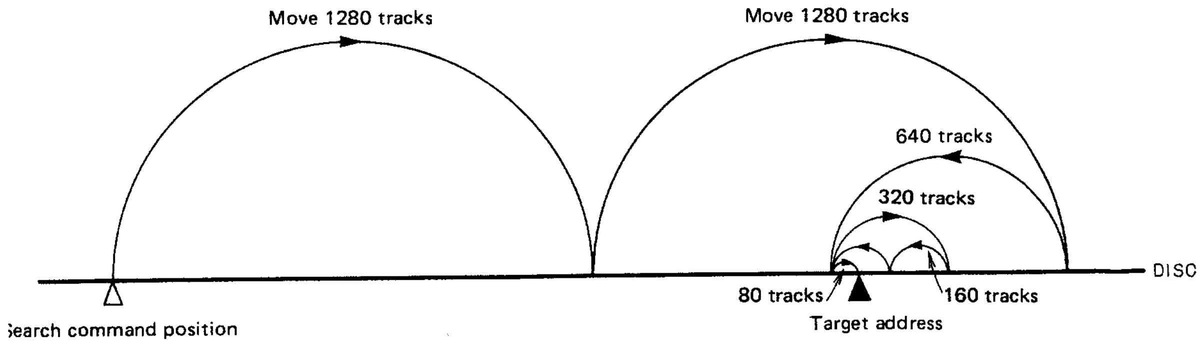


Fig. 32 Carriage Movement in Step Search (When distance to target address is unknown)

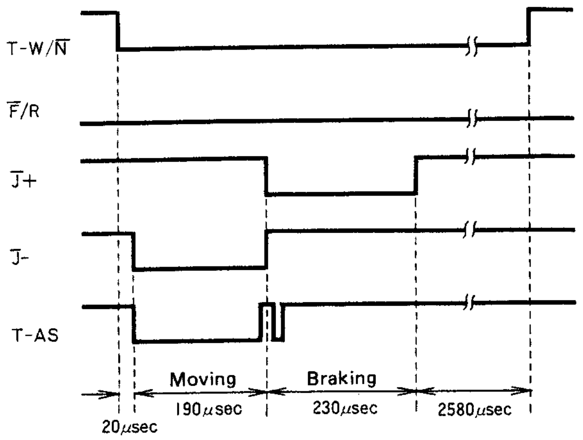


Fig. 33 FWD.I Track Jump

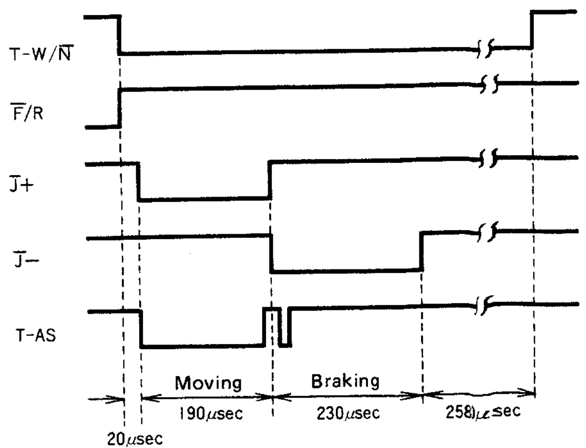


Fig. 34 REV.I Track Jump

• The Protective Functions During Search Operations

While the pickup is being moved, an erroneous movement may result if the pickup jumps out onto the mirror surface (outside the program area) of the disc. It is therefore necessary to be able to return the pickup quickly toward the center of the disc where data is recorded. For this purpose the state of FT (pin 16) is monitored at 1 msec intervals while the pickup is moving. If the FT signal becomes "L," it is assumed that the pickup has jumped outside of the mirror surface and the direction of the pickup movement is reversed (F/R of PD8010 (pin 15) becomes "H"). Monitoring of FT (pin 16) continues until it returns to "H." After counting 100 cross track pulses that enter DTE and confirming that the pickup has returned to a position containing data, the movement of the pickup is stopped, the address is read, and the search is continued.

In this operation, if FT (pin 16) does not return to "H" within 250 msec after the direction of pickup movement has been reversed, and if 100 DTE signals cannot be picked up, there may be a problem in the focus servo system; operation will be restarted from focus servo circuit activation (the setup mode).

If search is not completed after seven seconds, a time-out is provided to stop the pickup movement. This is a protective function in case there are problems in the mechanism for moving the pickup, or when normal pulses are no longer input by DTE (pin 18) and HFD (pin 10).

• Display During Search Mode

During the search mode, the display shows the track number of the target address and the words "DISC SET," flashing on and off. This display continues flashing until the unit finishes the search mode (until it finishes finding the address of the target and is ready to begin the play mode). The operational mode of the unit is visible on the display, as it is during the setup mode, making for easy visual verification.

5.7 PLAY MODE

This is the normal mode used when playing selections. As long as there are no special problems, all the sectors are monitored. The conditions of representative pins are as follows:

PD3023A		
Pin 19	$\overline{\text{MUT}}$	"H"
Pin 20	P/$\overline{\text{S}}$	"H"
Pin 22	T-$\overline{\text{N}}$/W	"L"
Pin 23	$\overline{\text{RA-G}}$	"H"
PD8010		
Pin 18	TAS	"H"
Pin 17	T-O/$\overline{\text{C}}$	"L"
Pin 16	R-O/$\overline{\text{C}}$	"H"
Pin 14	LOAD	"H"
Pin 13	$\overline{\text{PUSH}}$	"H"

In this mode a microcomputer monitors the address in the PLAY position obtained from the FT signal and the subcode every 13.3 msec. As explained before in the section on search mode protective measures in the search mode, this signal detects problems in the focus servo system and monitors the logic of the signal using FT of PD3023A (pin 16). If the level turns from "H" to "L," the microcomputer determines that there is a problem in the focus servo. The last address at which sound reproduction took place (i.e., immediately prior to the problem) is stored in the memory, and then the unit switches to the setup mode and restarts the focus servo circuit activation. After this the last address is located and the unit returns to the play mode.

The monitoring of the sound reproduction address is the greatest feature of this unit. When a sound skip occurs due to a sudden jolt or vibration, the pickup is returned immediately to the address just prior to the skip, in order to continue the play mode without interruption. This makes it possible to maintain continuous and smooth sound reproduction.

In actual operation, the next address to be read is constantly computed in PD3023A based on the reproduction address read during the play mode. When the next address is read, it is compared with the computed address. If there is more than a one-second difference between these two addresses, the units determines that for some other reason there has been a sound skip, and enters the search mode to locate the address derived through computation (called the expected value).

In the search mode the search operation is conducted to return the pickup to the previous address or to the expected address. Since the amount of sound skipped by a jolt, however, is generally no more than several seconds, the whole search operation usually takes no more than 0.5 seconds. After the search operation the unit resumes the play mode. To the user's ear, the sound stops for no more than a second before the playing resumes. For all practical purposes, sound reproduction takes place without interruption. This is the sound skip recovery operation by which the address of the sound reproduction is monitored. For this function to operate correctly, however, the subcode must be accurately read. Checks are perfomed to verify whether or not the subcode is being read during the Play mode. If 16 consecutive attempts to read the subcode fail, the unit returns to the setup mode in a manner similar to the FT monitoring function, and focusing operation. This means that during the play mode, the unit cannot become operational unless the normal subcode signals reach PD3023A pins 30, 31 and 39.

• Display During the Play Mode

During the play mode "DISC SET" and six digits indicating the track number, and minutes and seconds of play are lit up on the display. These numbers continue to count upwards as music reproduction progresses.

When the unit is engaged in the above-mentioned protective function, either "DISC SET" or "DISC SET" and "TNO" flash to indicate which mode the unit has gone into.

• Address Reading Using the Subcode

Demodulation of the Q channel of the subcode is performed in IC4 (TC9178F) inside the signal processing unit. It is capable of transmitting 80 bits in 20 groups of four bits. In this unit, however, the function of transmitting in four-bit groups is not used; instead, S0S1, SCQU, and PFCK are directly sent to PD3023A pins 30, 31 and 39 to perform the CRC check with PD3023A.

S0S1 is a synchronous signal that makes 98 bits of subcode one frame. SCQU is the control display data of subcode Q channel. These two signals are synchronous with the leading edge of the PFCK signal.

PD3023A detects the leading edge of PFCK through pin 39 and simultaneously checks the condition of S0S1 at pin 30. When pin 30 is "H," (i.e., from the moment it detects the synchronization of the frame) it synchronizes with the leading edge of PFCK and reads 96 bits of the SCQU data to perform the CRC check and take in the subcode. Since one cycle of the PFCK signal is 136 μs, and the subcode is composed of 98 bits of data including the sink pattern of S0 and S1, it requires approximately 13.3 msec to take in a subcode once.

5.8 PAUSE MODE

When the PAUSE/RELEASE button is pressed during the play mode, the unit goes into the pause mode. In the pause mode, two addresses are compared: the address of the pickup at the time the unit went into the pause mode and the address being currently read by the pickup. When the address being read currently is ahead, it performs a one-track reverse jump.

If the pickup is moved by some sudden jolt during the pause mode, the above-mentioned function goes into operation at the address where the pickup lands after the jolt. As a protective function during the pause mode, only FT check is conducted (as during the play mode).

After entering the pause mode the display is the same as during PLAY, and only the colon (:) between the minute and second digits blinks. The time display indicates the time at which the unit entered the pause mode.

5.9 FAST FORWARD AND REVERSE MODES

These functions resembles the fast forward and reverse functions in cassette decks. With FF (Fast Forward), the pickup jumps 20 tracks toward the outside edge and reads the subcode once. In the case of REV (Reverse), the operation is the same except that the pickup moves towards the center of the disc.

During this "20-track multi-jump operation," R-O/C PD8010 (pin 16) and RA-G PD3023A (pin 23) are both set at "L." Thus the carriage servo is given an offset to facilitate pickup movement. In this mode, when the lead-in area is reached through REV, or the lead-out area is reached through FF, the unit starts searching for the first selection. Then it resumes the play mode.

The display shows the same information as the play mode, but since the pickup is moving rapidly in the radial direction, the speed of counter increment is about twenty times as fast.

6. SERVICING INFORMATION

• Notes on Servicing the CD Player

1. Refer to the service manual when servicing the Pickup Unit (CGM-001). When replacing it, take measures to prevent static electricity damage (by protecting the unit with a short pin, etc.) and be sure to take all necessary precautions.
2. This CD Player monitors the internal temperature in the player section (PD6029 pin 8 TEMP), and in the hide-away section (PD3023A pin 17 TEMP). When the temperature in the unit rises and one of these circuits detects an "L," the unit goes into a hold condition with "H" output from POWER and AUXB of PD3023A. When this happens the display indicates "HH HHHH." (In this condition, only the loading and eject functions are operational.)
3. When the backup power source is not connected to this unit, it becomes impossible to reset the system controller (PD3023A), and the unit cannot be started.
4. When the inserted disc is dirty or has defects, or when it is upside down, this unit goes into the eject mode. When the eject operation is not finished within six seconds (including mechanical problems), the system controller brings all operations to a stop. In order to return to normal operation either:
    - press the clear button, or
    - switch the power off and back on.

   It is necessary to reset the system controller in this manner to start the unit back up.
5. When checking the basic functions of the various sections of this unit, put the system controller in the Test mode. (Refer to the Adjustment section in the Service Manual.)
6. When the CD player is powered and no disc is loaded, the amount of electricity consumed is approximately 100 mA. During the play mode, the normal electrical consumption is approximately 1.2 A. Pay attention to the voltmeter when switching the power on. If there is a current of more than 500 mA, shut the power off. (There are cases where this excessive current can increase the damage.)

• CD Player Test Mode Switch Functions

Note: In the test mode, the track number and time display both reset to zero. (00 TRACK NO. 00 MINUTE 00 SECOND)

No.	Switch name		Function	Display	Operation description	Comments
1	TRC TRACK		POWER: ON/OFF	ON: PLAY	Makes the PD3023A pin 18 ($\overline{\text{power}}$) "L," and starts the DC-DC converter.	
2	DSP DISPLAY		LD POWER : ON/OFF	ON : SET	Makes the PD6029 pin 1 ($\overline{\text{LD}}$) "L," and fires the laser diode.	It won't operate if NO. 1 (TRC) is not on.
3	SCAN SCAN		Spindle motor: ON/OFF	ON : DISC	Makes the PD3023A pin 20 (P/$\overline{\text{S}}$) "H," and turns the spindle motor.	It won't operate if NO. 1 (TRC) is not on.
4	RP REPEAT		Focus servo: OPEN/CLOSE	CLOSE : ART	Makes the PD8010 pin 13 ($\overline{\text{PUSH}}$) "H," and closes the focus servo loop.	It won't operate if NO. 1 (TRC) is not on.
5	REL/PAUSE		Tracking servo: OPEN/CLOSE	CLOSE : SCAN	Makes the PD8010 pin 17 (T-o/$\overline{\text{c}}$) "L," and closes the tracking servo loop.	Pushing this button once turns buttons one to four on changing the functions of the buttons. This stage persists until either the power is turned off or the clear button is pushed.
6	FF (+)	While playing	Forward jump	———	Outputs pulses to PD8010 pins 20 ($\overline{\text{J}}$-), 19 ($\overline{\text{J}}$+) and 18 (T-AS) [causing a forward jump].	Normally playing (test mode).
		While stopped.	Drives the carriage motor	———	Makes the PD8010 pin 15 ($\overline{\text{F}}$/R) "L," and outputs a pulse to pin 16 (R-O/$\overline{\text{C}}$) driving the carriage.	It won't operate if NO. 1 (TRC) is not on.
7	REV (–)	While playing	Reverse jump	———	Outputs pulses to PD8010 pins 20 ($\overline{\text{J}}$-) 19 ($\overline{\text{J}}$+) and 18 (T-AS)[causing a reverse jump].	Normally playing (test mode)
		While stopped.	Drives the carriage motor backward.	———	Makes the PD8010 pin 15 ($\overline{\text{F}}$/R) "H," and outputs a pulse to pin 16 (R-O/$\overline{\text{C}}$) driving the carriage.	It won't operate if NO. 1 (TRC) is not on.

5.8 PAUSE MODE

When the PAUSE/RELEASE button is pressed during the play mode, the unit goes into the pause mode. In the pause mode, two addresses are compared: the address of the pickup at the time the unit went into the pause mode and the address being currently read by the pickup. When the address being read currently is ahead, it performs a one-track reverse jump.

If the pickup is moved by some sudden jolt during the pause mode, the above-mentioned function goes into operation at the address where the pickup lands after the jolt. As a protective function during the pause mode, only FT check is conducted (as during the play mode).

After entering the pause mode the display is the same as during PLAY, and only the colon (:) between the minute and second digits blinks. The time display indicates the time at which the unit entered the pause mode.

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2. This CD Player monitors the internal temperature in the player section (PD6029 pin 8 TEMP), and in the hide-away section (PD3023A pin 17 TEMP). When the temperature in the unit rises and one of these circuits detects an "L," the unit goes into a hold condition with "H" output from POWER and AUXB of PD3023A. When this happens the display indicates "HH HHHH." (In this condition, only the loading and eject functions are operational.)
3. When the backup power source is not connected to this unit, it becomes impossible to reset the system controller (PD3023A), and the unit cannot be started.
4. When the inserted disc is dirty or has defects, or when it is upside down, this unit goes into the eject mode. When the eject operation is not finished within six seconds (including mechanical problems), the system controller brings all operations to a stop. In order to return to normal operation either:
    - press the clear button, or
    - switch the power off and back on.

   It is necessary to reset the system controller in this manner to start the unit back up.
5. When checking the basic functions of the various sections of this unit, put the system controller in the Test mode. (Refer to the Adjustment section in the Service Manual.)
6. When the CD player is powered and no disc is loaded, the amount of electricity consumed is approximately 100 mA. During the play mode, the normal electrical consumption is approximately 1.2 A. Pay attention to the voltmeter when switching the power on. If there is a current of more than 500 mA, shut the power off. (There are cases where this excessive current can increase the damage.)

• CD Player Test Mode Switch Functions

Note: In the test mode, the track number and time display both reset to zero.

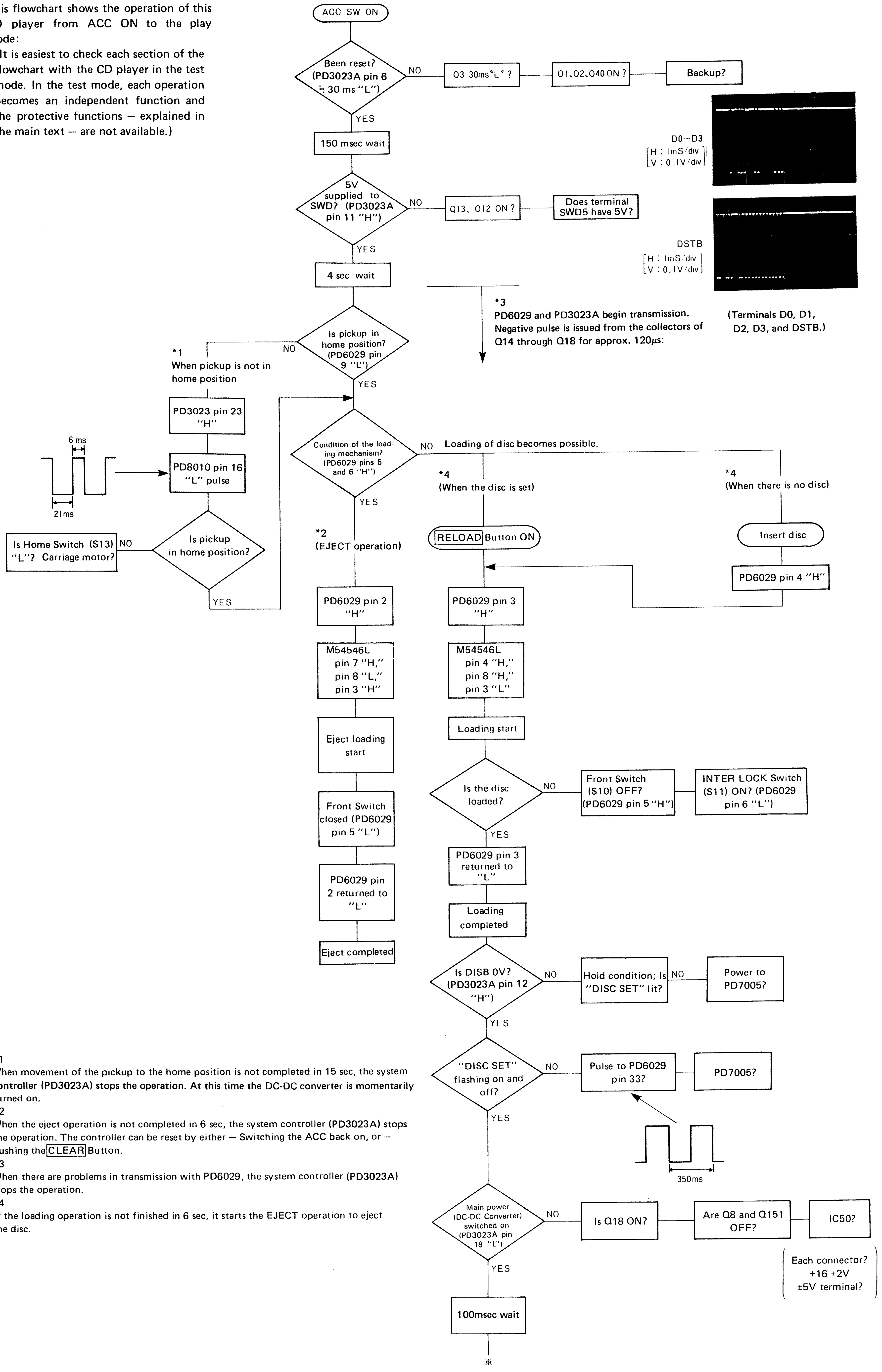
00	00	00
TRACK NO.	MINUTE	SECOND

No.	Switch name		Function	Display	Operation description	Comments
1	TRC TRACK		POWER: ON/OFF	ON: PLAY	Makes the PD3023A pin 18 ($\overline{\text{power}}$) "L," and starts the DC-DC converter.	
2	DSP DISPLAY		LD POWER : ON/OFF	ON : SET	Makes the PD6029 pin 1 ($\overline{\text{LD}}$) "L," and fires the laser diode.	It won't operate if NO.1 (TRC) is not on.
3	SCAN SCAN		Spindle motor: ON/OFF	ON : DISC	Makes the PD3023A pin 20 (P/$\overline{\text{S}}$) "H," and turns the spindle motor.	It won't operate if NO.1 (TRC) is not on.
4	RP REPEAT		Focus servo: OPEN/CLOSE	CLOSE : ART	Makes the PD8010 pin 13 ($\overline{\text{PUSH}}$) "H," and closes the focus servo loop.	It won't operate if NO.1 (TRC) is not on.
5	REL/PAUSE		Tracking servo: OPEN/CLOSE	CLOSE : SCAN	Makes the PD8010 pin 17 (T-o/$\bar{\text{c}}$) "L," and closes the tracking servo loop.	Pushing this button once turns buttons one to four on changing the functions of the buttons. This stage persists until either the power is turned off or the clear button is pushed.
6	FF (+)	While playing	Forward jump	———	Outputs pulses to PD8010 pins 20 ($\bar{\text{J}}$-), 19 ($\bar{\text{J}}$+) and 18 (T-AS) [causing a forward jump].	Normally playing (test mode).
		While stopped.	Drives the carriage motor	———	Makes the PD8010 pin 15 ($\overline{\text{F}}$/R) "L," and outputs a pulse to pin 16 (R-O/$\overline{\text{C}}$) driving the carriage.	It won't operate if NO.1 (TRC) is not on.
7	REV (–)	While playing	Reverse jump	———	Outputs pulses to PD8010 pins 20 ($\bar{\text{J}}$-) 19 ($\bar{\text{J}}$+) and 18 (T-AS)[causing a reverse jump].	Normally playing (test mode)
		While stopped.	Drives the carriage motor backward.	———	Makes the PD8010 pin 15 ($\overline{\text{F}}$/R) "H," and outputs a pulse to pin 16 (R-O/$\overline{\text{C}}$) driving the carriage.	It won't operate if NO.1 (TRC) is not on.

• Flowchart of CD Player From ACC ON to PLAY

This flowchart shows the operation of this CD player from ACC ON to the play mode:

(It is easiest to check each section of the flowchart with the CD player in the test mode. In the test mode, each operation becomes an independent function and the protective functions – explained in the main text – are not available.)

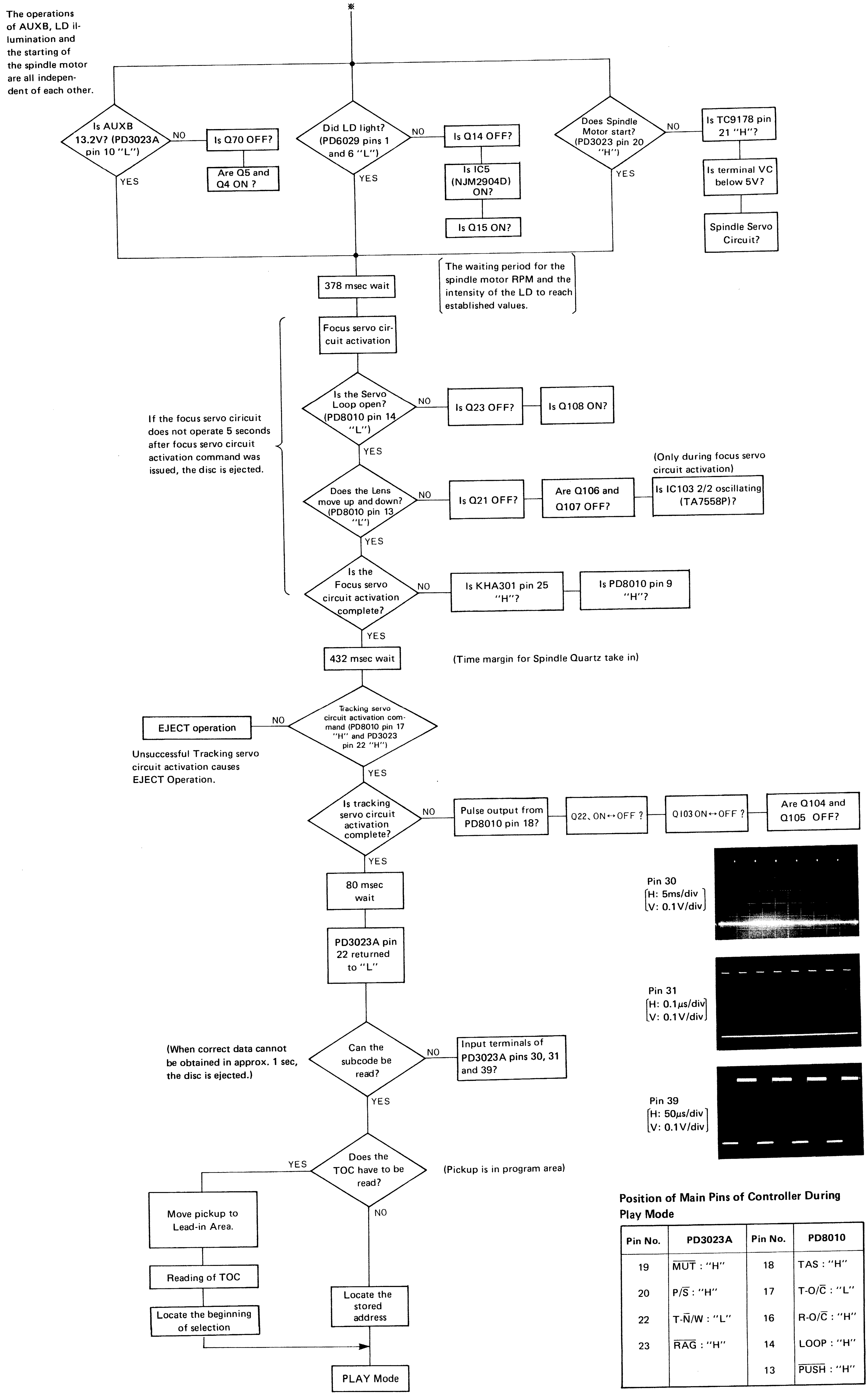

ACC SW ON
Been reset? (PD3023A pin 6 ≒ 30 ms "L")
NO
Q3 30ms"L" ?
Q1、Q2、Q40 ON ?
Backup?
YES
150 msec wait
D0~D3
H : 1mS/div
V : 0.1V/div
5V supplied to SWD? (PD3023A pin 11 "H")
NO
Q13、Q12 ON ?
Does terminal SWD5 have 5V?
YES
DSTB
H : 1mS/div
V : 0.1V/div
4 sec wait
*3
PD6029 and PD3023A begin transmission. Negative pulse is issued from the collectors of Q14 through Q18 for approx. 120μs.
(Terminals D0, D1, D2, D3, and DSTB.)
Is pickup in home position? (PD6029 pin 9 "L")
NO
*1
When pickup is not in home position
YES
PD3023 pin 23 "H"
6 ms
21ms
PD8010 pin 16 "L" pulse
Is pickup in home position?
NO
Is Home Switch (S13) "L"? Carriage motor?
YES
Condition of the loading mechanism? (PD6029 pins 5 and 6 "H")
NO
Loading of disc becomes possible.
*4
(When the disc is set)
*4
(When there is no disc)
YES
*2
(EJECT operation)
RELOAD Button ON
Insert disc
PD6029 pin 4 "H"
PD6029 pin 2 "H"
PD6029 pin 3 "H"
M54546L pin 7 "H," pin 8 "L," pin 3 "H"
M54546L pin 4 "H," pin 8 "H," pin 3 "L"
Eject loading start
Loading start
Is the disc loaded?
NO
Front Switch (S10) OFF? (PD6029 pin 5 "H")
INTER LOCK Switch (S11) ON? (PD6029 pin 6 "L")
Front Switch closed (PD6029 pin 5 "L")
YES
PD6029 pin 3 returned to "L"
PD6029 pin 2 returned to "L"
Loading completed
Eject completed
Is DISB 0V? (PD3023A pin 12 "H")
NO
Hold condition; Is "DISC SET" lit?
NO
Power to PD7005?
YES
"DISC SET" flashing on and off?
NO
Pulse to PD6029 pin 33?
PD7005?
350ms
YES
Main power (DC-DC Converter) switched on (PD3023A pin 18 "L")
NO
Is Q18 ON?
Are Q8 and Q151 OFF?
IC50?
Each connector? +16 ±2V ±5V terminal?
YES
100msec wait
※

*1
When movement of the pickup to the home position is not completed in 15 sec, the system controller (PD3023A) stops the operation. At this time the DC-DC converter is momentarily turned on.

*2
When the eject operation is not completed in 6 sec, the system controller (PD3023A) stops the operation. The controller can be reset by either – Switching the ACC back on, or – Pushing the CLEAR Button.

*3
When there are problems in transmission with PD6029, the system controller (PD3023A) stops the operation.

*4
If the loading operation is not finished in 6 sec, it starts the EJECT operation to eject the disc.


The operations of AUXB, LD illumination and the starting of the spindle motor are all independent of each other.
※
Is AUXB 13.2V? (PD3023A pin 10 "L")
NO
Is Q70 OFF?
Are Q5 and Q4 ON ?
YES
Did LD light? (PD6029 pins 1 and 6 "L")
NO
Is Q14 OFF?
Is IC5 (NJM2904D) ON?
Is Q15 ON?
YES
Does Spindle Motor start? (PD3023 pin 20 "H")
NO
Is TC9178 pin 21 "H"?
Is terminal VC below 5V?
Spindle Servo Circuit?
YES
378 msec wait
The waiting period for the spindle motor RPM and the intensity of the LD to reach established values.
Focus servo circuit activation
If the focus servo ciricuit does not operate 5 seconds after focus servo circuit activation command was issued, the disc is ejected.
Is the Servo Loop open? (PD8010 pin 14 "L")
NO
Is Q23 OFF?
Is Q108 ON?
YES
Does the Lens move up and down? (PD8010 pin 13 "L")
NO
Is Q21 OFF?
Are Q106 and Q107 OFF?
(Only during focus servo circuit activation)
Is IC103 2/2 oscillating (TA7558P)?
YES
Is the Focus servo circuit activation complete?
NO
Is KHA301 pin 25 "H"?
Is PD8010 pin 9 "H"?
YES
432 msec wait
(Time margin for Spindle Quartz take in)
Tracking servo circuit activation command (PD8010 pin 17 "H" and PD3023 pin 22 "H")
NO
EJECT operation
Unsuccessful Tracking servo circuit activation causes EJECT Operation.
YES
Is tracking servo circuit activation complete?
NO
Pulse output from PD8010 pin 18?
Q22、ON↔OFF ?
Q103 ON↔OFF ?
Are Q104 and Q105 OFF?
Pin 30 [H: 5ms/div V: 0.1V/div]
Pin 31 [H: 0.1μs/div V: 0.1V/div]
Pin 39 [H: 50μs/div V: 0.1V/div]
YES
80 msec wait
PD3023A pin 22 returned to "L"
Can the subcode be read?
(When correct data cannot be obtained in approx. 1 sec, the disc is ejected.)
NO
Input terminals of PD3023A pins 30, 31 and 39?
YES
Does the TOC have to be read?
(Pickup is in program area)
YES
Move pickup to Lead-in Area.
Reading of TOC
Locate the beginning of selection
NO
Locate the stored address
PLAY Mode

Position of Main Pins of Controller During Play Mode

Pin No.	PD3023A	Pin No.	PD8010
19	$\overline{\text{MUT}}$: "H"	18	TAS : "H"
20	P/$\overline{\text{S}}$: "H"	17	T-O/$\overline{\text{C}}$: "L"
22	T-$\overline{\text{N}}$/W : "L"	16	R-O/$\overline{\text{C}}$: "H"
23	$\overline{\text{RAG}}$: "H"	14	LOOP : "H"
		13	$\overline{\text{PUSH}}$: "H"